Integrated circuits

Book IC03N 1985
New series

Integrated circuits for telephony

INTEGRATED CIRCUITS FOR TELEPHONY

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

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Product specialists are at your service and enquiries will be answered promptly.

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks comprises:

T1 **Tubes for r.f. heating**

T2a **Transmitting tubes for communications, glass types**

T2b **Transmitting tubes for communications, ceramic types**

T3 **Klystrons, travelling-wave tubes, microwave diodes**

ET3 **Special Quality tubes, miscellaneous devices** (will not be reprinted)

T4 **Magnetrons for microwave heating**

T5 **Cathode-ray tubes**
Instrument tubes, monitor and display tubes, C.R. tubes for special applications

T6 **Geiger-Müller tubes**

T7 **Gas-filled tubes**
Segment indicator tubes, indicator tubes, dry reed contact units, thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes, associated accessories

T8 **Picture tubes and components**
Colour TV picture tubes, black and white TV picture tubes, colour monitor tubes for data graphic display, monochrome monitor tubes for data graphic display, components for colour television, components for black and white television and monochrome data graphic display

T9 **Photo and electron multipliers**
Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates

T10 **Camera tubes and accessories**

T11 **Microwave semiconductors and components**

T12 **Vidicons and Newvicons**

T13 **Image intensifiers**

T14 **Infrared detectors**

T15 **Dry reed switches**

Data collations on these subjects are available now. Data Handbooks will be published in 1985.

T16 **Monochrome tubes and deflection units**
Black and white TV picture tubes, monochrome data graphic display tubes, deflection units

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

S1 **Diodes**
Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes

S2a **Power diodes**

S2b **Thyristors and triacs**

S3 **Small-signal transistors**

S4a **Low-frequency power transistors and hybrid modules**

S4b **High-voltage and switching power transistors**

S5 **Field-effect transistors**

S6 **R.F. power transistors and modules**

S7 **Surface mounted semiconductors**

S8 **Devices for optoelectronics**
Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.

S9 **Power MOS transistors**

S10 **Wideband transistors and wideband hybrid IC modules**

S11 **Microwave semiconductors** (to be published in this series in 1985)
At present available in Handbook T11

S12 **Surface acoustic wave devices**

INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks comprises:

EXISTING SERIES

IC1 **Bipolar ICs for radio and audio equipment**

IC2 **Bipolar ICs for video equipment**

IC3 **ICs for digital systems in radio, audio and video equipment**

IC4 **Digital integrated circuits**
CMOS HE4000B family

IC5 **Digital integrated circuits – ECL** (superseded by IC08N)
ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs

IC6 **Professional analogue integrated circuits**

IC7 **Signetics bipolar memories**

IC8 **Signetics analogue circuits**

IC9 **Signetics TTL logic** (superseded by IC09N and IC15N)

IC10 **Signetics Integrated Fuse Logic (IFL)**

IC11 **Microprocessors, microcomputers and peripheral circuitry**

NEW SERIES

IC01N	**Radio, audio and associated systems** Bipolar, MOS	
IC02N	**Video and associated systems** Bipolar, MOS	
IC03N	**Integrated circuits for telephony** Bipolar, MOS	(published 1985)
IC04N	**HE4000B logic family** CMOS	
IC05N	**HE4000B logic family uncased integrated circuits** CMOS	(published 1984)
IC06N	**PC54/74HC/HCU/HCT logic families** HCMOS	
IC07N	**PC54/74HC/HCU/HCT uncased integrated circuits** HCMOS	
IC08N	**10K and 100K logic family** ECL	(published 1984)
IC09N	**Logic series** TTL	(published 1984)
IC10N	**Memories** MOS, TTL, ECL	
IC11N	**Linear LSI**	(published 1985)
IC12N	**Semi-custom gate arrays & cell libraries** ISL, ECL, CMOS	
IC13N	**Semi-custom integrated fuse logic** IFL series 20/24/28	
IC14N	**Microprocessors, microcontrollers & peripherals** Bipolar, MOS	
IC15N	**Logic series** FAST TTL	(published 1984)

Note

Books available in the new series are shown with their date of publication.

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

C1 **Programmable controller modules**
PLC modules, PC20 modules

C2 **Television tuners, video modulators, surface acoustic wave filters**

C3 **Loudspeakers**

C4 **Ferroxcube potcores, square cores and cross cores**

C5 **Ferroxcube for power, audio/video and accelerators**

C6 **Synchronous motors and gearboxes**

C7 **Variable capacitors**

C8 **Variable mains transformers**

C9 **Piezoelectric quartz devices**
Quartz crystal units, temperature compensated crystal oscillators, compact integrated oscillators, quartz crystal cuts for temperature measurements

C10 **Connectors**

C11 **Non-linear resistors**
Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)

C12 **Variable resistors and test switches**

C13 **Fixed resistors**

C14 **Electrolytic and solid capacitors**

C15 **Ceramic capacitors***

C16 **Permanent magnet materials**

C17 **Stepping motors and associated electronics**

C18 **D.C. motors**

C19 **Piezoelectric ceramics**

C20 **Wire-wound components for TVs and monitors**

C21 **Assemblies for industrial use**
HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices

* Film capacitors are included in Data Handbook C22 which will be published in 1985. The September 1982 edition of C15 should be retained until C22 is issued.

INTRODUCTION

INTRODUCTION

In the past decade advances in microcircuit technology have resulted in the development of microprocessors, memories, and dedicated ICs that are now replacing traditional components of the subscriber set, to the benefit of both its performance and appearance.

As an example, ICs for interrupted current-loop dialling (decadic or pulse) and for dual-tone multi-frequency (DTMF) dialling allow the dial to be replaced by a push-button keyboard. Also, by replacing the carbon microphone with an active type (electret or electro-dynamic) and using an electronic anti-sidetone circuit, the speech and transmission functions can be performed by an integrated circuit. Speech and dialling functions can now be integrated into one chip, and the bell will eventually be replaced by an electronically-driven transducer with a variety of ringing tones.

Integrated circuits also allow incorporation of a host of new features, such as automatic redialling, repertory dialling, automatic emergency-call dialling, dialled number display, tariff-unit metering, speech synthesising, loudspeaking and cordless telephones, and possibly a limited amount of data handling.

Research is also progressing into an Integrated Services Digital Network (ISDN) in which digitized voice, circuit-switched data and digital signalling, combined with packet switched data, can be processed. This trend will lead to the development of ICs for interface and protocol functions (firstly in office communication systems, and eventually in public networks).

The long life of existing equipment together with the fact that its manufacture is often automated, means that several years must elapse before new components can prove their operational and economic superiority to the telephone authorities. Many of the new components will therefore have to work alongside the old ones, and the order and speed of approach to all-electronic subscriber equipment will not necessarily be the same in all countries. Because of this we are producing and developing a wide range of integrated circuits for telephones of the present and for those of the future.

SELECTION GUIDE

Numerical index
Functional index
Pulse diallers with redial, PCD3320 family
Transmission circuits TEA1042, TEA1060, TEA1061

NUMERICAL INDEX

type number	brief description	pins	package code *	I^2C bus	page
CMOS					
PCD3310	pulse and DTMF dialler with redial	20	P		25
		28	T		25
PCD3311	DTMF generator with serial I/O	14	P	•	29
	and parallel data input	16	T	•	29
PCD3312	DTMF generator with serial I/O	8	P	•	29
		8	T	•	29
PCD3315	ten-number repertory dialler with redial	28	P,T		47
PCD3320	pulse diallers with redial (see section guide, page 10)	18	P,D		53
PCD3321		18	P,D		61
PCD3322		18	P,D		83
PCD3323		28	P,D,T		97
PCD3324		18	P,D		117
PCD3325A		18	P		133
PCD3326		18	P		149
PCD3343	microcontroller for telephone sets	28	P,D,T	•	165
PCD3360	programmable multi-tone ringer	16	P,T		205
PCD3361	programmable multi-tone ringer	8	P,T		205
PCD5101	256 x 4-bit static RAM	22	P		219
		24	T		219
PCD5114	1024 x 4-bit static RAM	18	P,D		227
		20	T		227
PCD8571	128 x 8-bit static RAM with serial I/O	8	P,D,T	•	235
PCF1251	micropower voltage detector	8	P,T		247
PCF2111	LCD duplex driver (64 segments)	40	P,T		251
PCF8570	256 x 8-bit static RAM with serial I/O	8	P	•	261
PCF8573	clock/calendar with serial I/O	16	P	•	273
PCF8574	remote 8-bit I/O expander for I^2C bus systems	16	P,T	•	291
PCF8576	1:4 MUX LCD driver with serial I/O	56	T,U	•	303
PCF8577	1:2 MUX LCD driver with serial I/O	40	P,T	•	335

type number	brief description	pins	package code *	I^2C bus	page
BIPOLAR					
TDA7000	FM radio receiver	18	P		351
TDA7050	dual audio amplifier for line-powered speaker-phones	8	T		359
TEA1042▲	transmission circuit for speaker-phone	24	P		363
TEA1046	DTMF dialler and transmission circuit	24	P		377
TEA1060▲	transmission circuit with dialler interface: low-impedance input for dynamic and magnetic microphones	18	P		391
TEA1061▲	transmission circuit with dialler interface: high-impedance input for electret and piezo-electric microphones	18	P		391
TEA1075	DTMF dialler with line interface and mute switch	18	P		405

* Add the package code suffix to all orders.
D: ceramic (cerdip) package (DIL); P: plastic package (DIL); T: plastic mini-pack (SO, VSO) for surface-mounting; U: uncased integrated circuit.

▲ See selection guide, page 12.

FUNCTIONAL INDEX

PULSE DIALLERS WITH REDIAL, PCD3320 FAMILY

parameter	PCD						
	3320	3321	3322	3323	3324	3325A	3326
Number of pins	18	18	18	28	18	18	18
Dialling pulse frequency 10 Hz	●	●	●	●	●	●	●
selectable with F01, F02 16, 20 Hz		●		●	●	●	●
Mark/space ratio 3:2	●	●	●	●	●	●	●
selectable with M/S 2:1		●		●	●	●	●
Interdigit pause duration $8 \times T_{DP}$	●	●	●	●	●	●	●
selectable with IDP $9 \times T_{DP}$				●			
Reset delay for line power breaks $1{,}6 \times T_{DP}$	●	●	●	●	●	●	●
selectable with RDS $3{,}2 \times T_{DP}$				●			
Access pauses repeated during redial		●		●	●	●	●
Manual insertion of access pauses		●		●	●	●	●
Automatic access pause insertion: max. 1					●		
max. 2		●		●			●
Access pause duration $32 \times T_{DP}$		●		●	●		●
selectable with APD $64 \times T_{DP}$				●			●
not automatically terminated						●	
$\overline{M1}$, inverted mute output	●		●	●			
M2, strobe output			●	●			
M3, AND function of mute (M1) and inverted dialling pulse ($\overline{DP}$) outputs	●			●			
CL, clock output				●			
APO, access pause output				●			
HOLD, dialling-interrupt input				●			
APO+HOLD, internally connected		●			●	●	●
APR, access pause reset input				●			
AAE, automatic access pause enable				●			
APD, access pause duration selection input				●			●

T_{DP} = dialling pulse period.

Features common to all PCD3320 family

OSC IN
OSC OUT } on-chip oscillator input and output

X1 to X3, column keyboard inputs with on-chip pull-down

Y1 to Y4, row keyboard inputs with on-chip pull-up

CE, chip enable input

DP, dialling pulse drive output to external line-switching transistor or relay

M1, muting output

TRANSMISSION CIRCUITS TEA1042, TEA1060, TEA1061

parameter	TEA1042	TEA1060	TEA1061
Microphone inputs:			
low sensitivity – dynamic or magnetic		●	
medium sensitivity – dynamic or magnetic	●	●	
electret with source follower			●
electret with preamplifier	●		●
electret with preamplifier (loudspeaker)	●		
piezo-electric			●
Receiver outputs:			
dynamic or magnetic	●	●	●
piezo-electric		●	●
output for loudspeaker amplifier	●		
Mode switch, handset/loudspeaker	●		
Electronic mute input	●	●	●
DTMF input	●	●	●
Voltage regulator:			
adjustable d.c. voltage	●		
adjustable d.c. resistance	●	●	●
Power-down input		●	●
Gain control:			
control can be switched off	●	●	●
adapted to 400 Ω feed	●		
adapted to 600 Ω feed		●	●
adapted to 800 Ω feed	●		
adaptable to exchange supply voltage	●	●	●

ARCHITECTURE OF ELECTRONIC SUBSCRIBER SETS

Telephones for pulse dialling
Telephones for DTMF dialling

ARCHITECTURE OF ELECTRONIC SUBSCRIBER SETS

The first step in converting subscriber sets to electronic operation is usually in the replacement of the rotary dial by a push-button keyboard operating with a pulse generator for interrupted current-loop dialling, or with a tone generator for DTMF dialling. This effectively divides electronic telephone production into two main streams – one for pulse dialling and one for tone dialling. Subsequent steps are in the replacement of the carbon microphone by an active transducer such as an electret or electro-dynamic microphone, and replacement of the transformer hybrid by an integrated speech/transmission circuit. The sequence continues with the inclusion of features such as repertory dialling, last-number redial, extended redial, dialled number display, and tariff-unit metering. Some sets will also have the capability of either pulse or DTMF dialling.

The ringer is a completely separate function and can therefore be replaced by electronics at any stage.

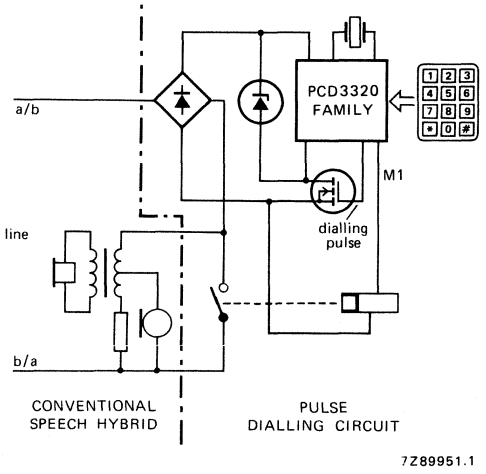
Telephones for pulse dialling

Fig. 1 shows the architecture of basic push-button subscriber sets for interrupted current-loop dialling using the PCD3320 family of ICs.

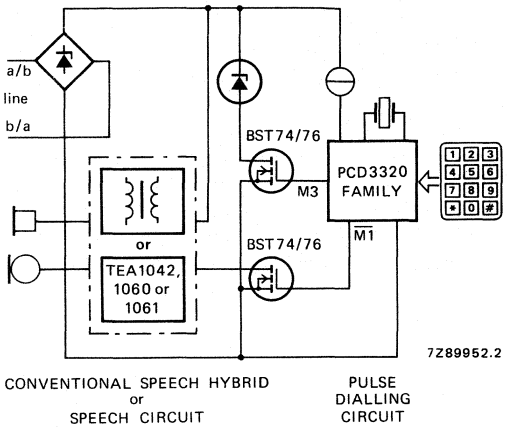
In Fig. 1(a), an insert unit to perform the dial function is shown in a conventional set with a transformer hybrid. A muting relay inhibits the speech function during dialling.

Fig. 1(b) shows a parallel circuit in which the line current flows through either the speech part or a dummy load and is interrupted by the M3 output of the dialling IC. Note that the conventional speech circuit operating with two wires may be replaced by a speech/transmission circuit (TEA1060/1061); this allows the possibility of operating the speech IC in the handset with only a two-wire cable.

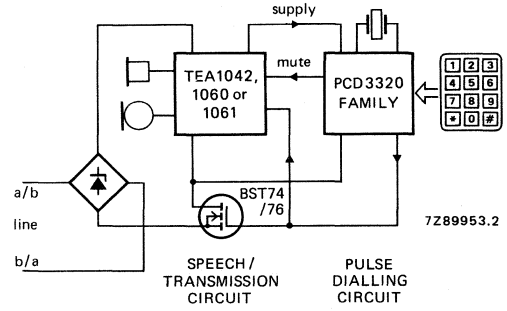
In Fig. 1(c), the dialling IC operates in conjunction with a transmission IC with common-line interface. The latter works with either an electret or an electro-dynamic microphone and has a special input for muting. For this function we have three speech/transmission ICs (TEA1042, 1060 and 1061).



(a) Pulse dial insert unit replacing the rotary dial in a conventional telephone set.



(b) Pulse dial basic set with either conventional or electronic speech.



(c) Pulse dial basic set with two ICs and common line interface.

Fig. 1 Subscriber set architecture for current loop dialling (ringer cradle contact, polarity guard and protection not shown).

Telephones for DTMF dialling

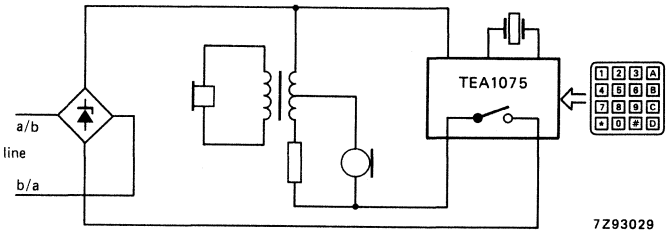
Fig. 2 shows the architecture of four basic push-button sets for DTMF dialling.

In Fig. 2(a) a conventional speech circuit with a transformer hybrid is used together with a DTMF generator; this requires a DTMF generator which has an output stage, line interface and mute switch.

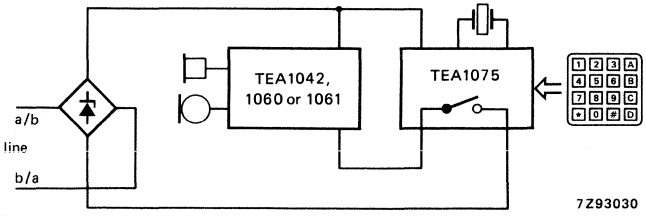
Fig. 2(b) shows the same DTMF generator applied with an electronic speech circuit. Both DTMF generator and speech circuit have interfaces to the line.

In Fig. 2(c) only the speech circuit interfaces to the line. The DTMF generator is connected to the speech circuit which has a DTMF and a mute input for this purpose. The speech circuit incorporates a voltage stabilizer and audio output stage for both speech and DTMF signals. Note that the speech ICs in this application are the same as used for the pulse dial application shown in Fig. 1(c).

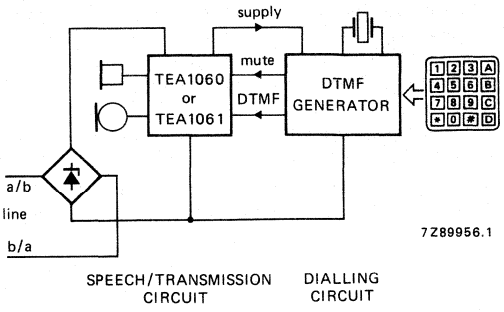
The application of a combined DTMF/transmission circuit (TEA1046) is shown in Fig. 2(d).



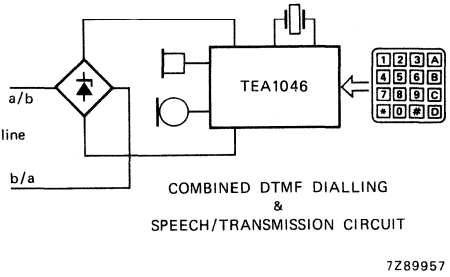
(a) DTMF set using a conventional speech circuit.



(b) Full electronic DTMF set.



(c) DTMF basic set with two ICs and common line interface.



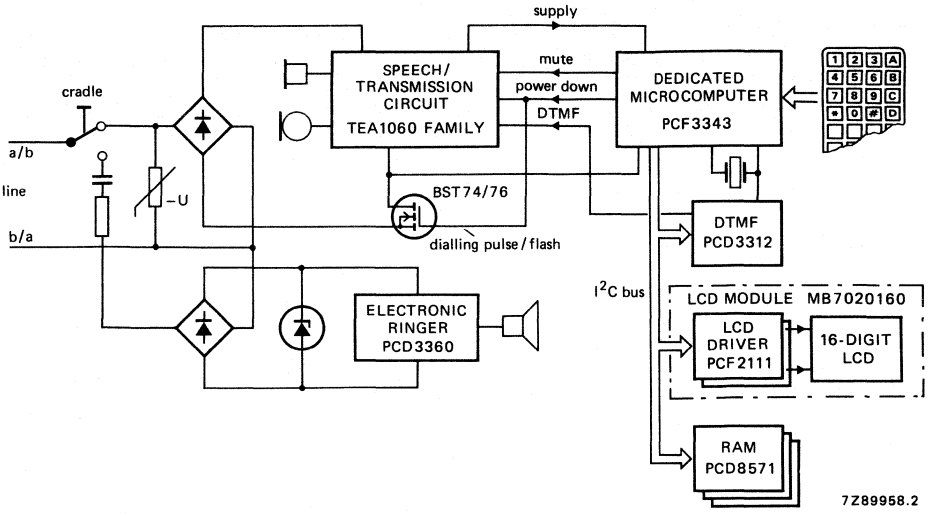
(d) Electronic speech and DTMF on a single chip.

Fig. 2 Subscriber set architecture for dual-tone multi-frequency (DTMF) dialling (ringer, cradle contact, polarity guard and protection not shown).

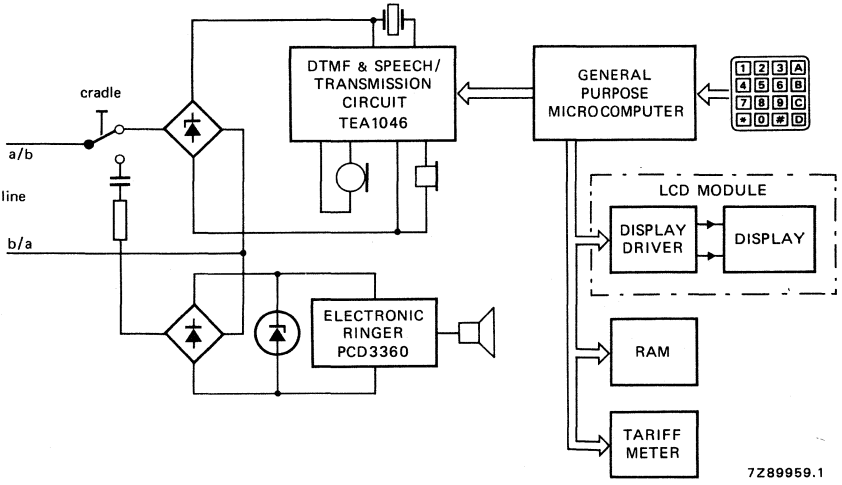
Multi-feature telephones

The subscriber set shown in Fig. 3(a) has added features including last-number redial, extended redial, repertory dialling, register recall and dialled-number display. The PCF3343 telephone microcontroller shown in this example interfaces with the I^2C bus – a two-wire serial input/output data bus. The I^2C bus allows peripheral devices to be added, such as up to eight CMOS RAMs (PCD8571) to augment the ten 16-digit numbers which can be stored on-chip in the PCF3343. Other additions may be an LCD driver (PCF2111), a clock/timer circuit (PCF8573) and DTMF generator (PCD3312). A DTMF generator (PCD3311) which operates with a 4 or 8-bit microcontroller is also available.

Fig. 3(b) shows a variation using a general-purpose microcomputer with parallel input/output in conjunction with the TEA1046 DTMF/speech/transmission IC (which has microcomputer-compatible keyboard inputs).



(a) Feature-phone using dedicated microcontroller PCF3343.



(b) Variation using a general-purpose microcomputer with parallel input/output.

Fig. 3 Multi-feature subscriber set architecture.

Cordless telephones

Our dedicated telephony ICs will enhance any attractive mobile telephone design. A concept of a cordless telephone operating with carrier frequencies of 46/49 MHz (FCC standards) is shown in Fig. 4. The remote handset has a 46 MHz FM receiver (TDA7000), a pulse dialler (PCD332X) and an earpiece/loudspeaker amplifier (TDA7050). The base unit has a 49 MHz FM receiver (TDA7000), a telephone line transmission circuit (TEA1060/61) and a ring-detector/ring-generator (PCD3360).

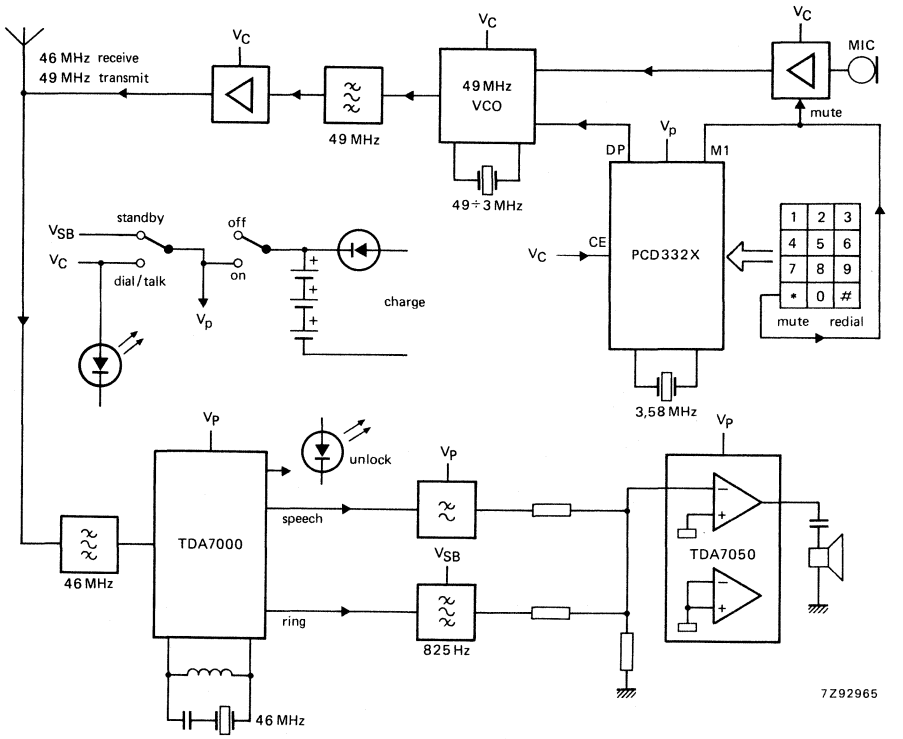


Fig. 4(a) Remote unit for pulse dialling cordless telephones.

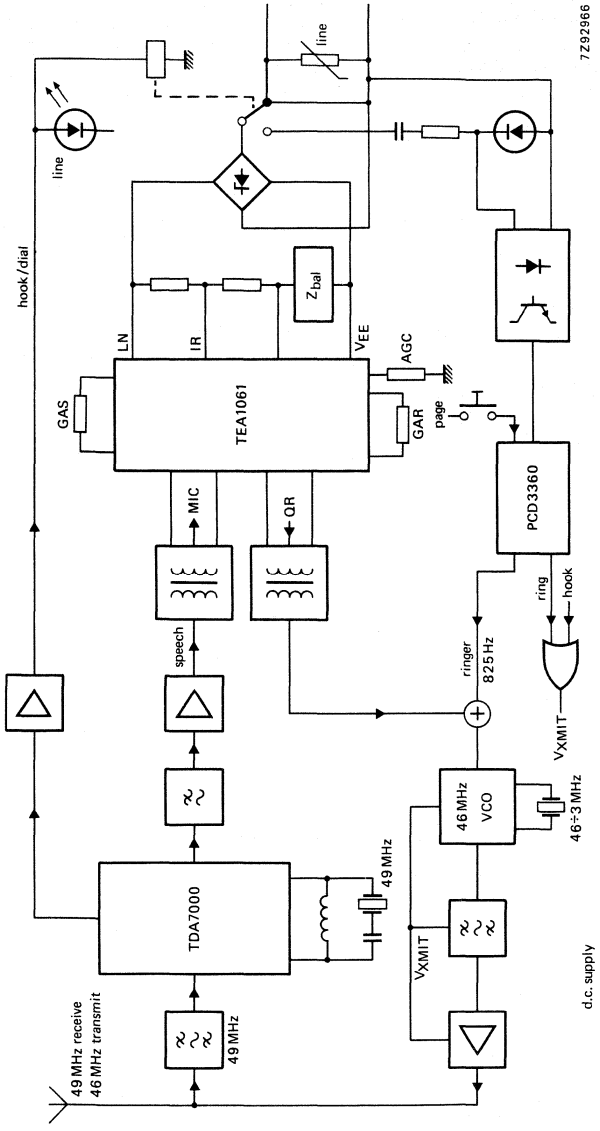


Fig. 4(b) Base unit for pulse dialling cordless telephones.

Speaker-phone

The "speaker-phone" has a base unit which amplifies received speech and speech for transmission without using the traditional handset, and is ideal for conference and other hands-free applications. An outline of the system is shown in Fig. 5, this uses a specially developed IC, the TEA1042, which has double transmission and receiving amplifiers. Increased gains in the send and receive channels can be achieved without instability by the introduction of complementary-driven attenuators (VS1, VS2) in the speech channels.

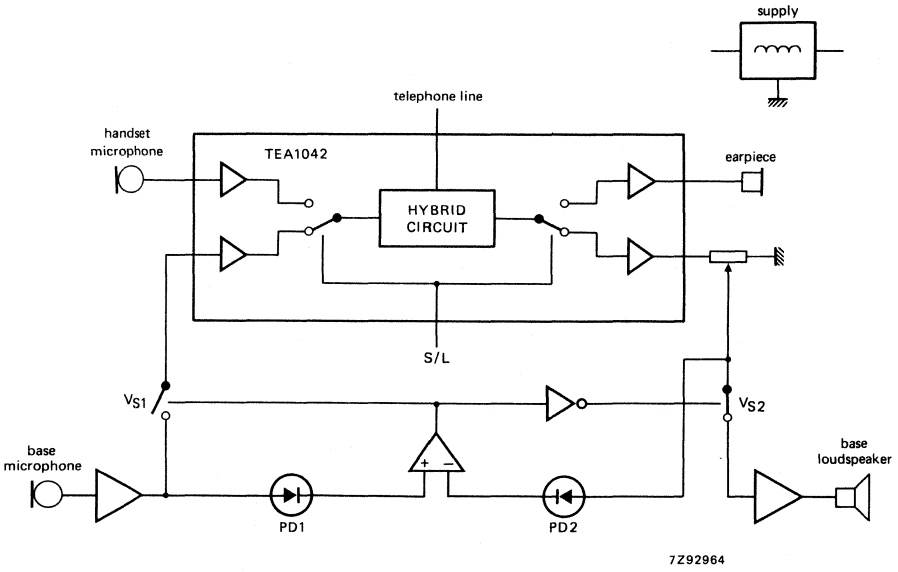


Fig. 5 Basic speaker-phone system.

DEVICE DATA

PULSE AND DTMF DIALLER WITH REDIAL

GENERAL DESCRIPTION

The PCD3310 is a single-chip silicon gate CMOS integrated circuit with an on-chip oscillator for a 3,58 MHz crystal. It is a dual-standard dialling circuit for either pulse dialling (PD) or dual tone multi-frequency (DTMF) dialling.

Input data is derived from any standard matrix keypad for dialling in either PD or DTMF mode. Numbers of up to 23 digits can be retained in RAM for redial and notepad facilities.

In DTMF mode bursts as well as pauses are timed to a minimum, in manual dialling the maximum depends on the key depression time.

Features

- Pulse and DTMF dialling
- 23-digit capacity for redial operation (cursor method)
- Memory clear and electronic notepad
- Mixed mode dialling; start with PD and end with DTMF dialling
- Dual redial buffers for PABX and public calls
- Four extra function keys; program, flash, redial, PD to DTMF (mixed dialling)
- DTMF timing:
  - manual dialling - minimum duration for bursts and pauses
  - redialling - calibrated timing
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)
- On-chip oscillator uses low-cost 3,58 MHz (tv colour burst) crystal
- Uses standard single-contact or double-contact (common left open) keypad
- Keyboard entries fully debounced at both edges
- Flash (register recall) output

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}		2,5 to 6,0 V
Standby supply voltage	V_{DDO}		1,8 to 6,0 V
Low standby current (on hook) at V_{DDO} = 1,8 V	I_{DDOmax}		5 μA
Operating currents at V_{DD} = 3,0 V			
conversation mode	I_{DDC}	max.	60 μA
pulse dialling mode	I_{DDP}	max.	200 μA
DTMF dialling mode	I_{DDF}	max.	1,2 mA
DTMF voltage levels (r.m.s. values)	$V_{tone(rms)}$		150 and 192 mV
Pre-emphasis	ΔV		2,1 dB
Total harmonic distortion	d_{tot}		−25 dB
Operating ambient temperature range	T_{amb}		−25 to +70 °C

PACKAGE OUTLINES

PCD3310P: 20-lead DIL; plastic (SOT-146).
PCD3310T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

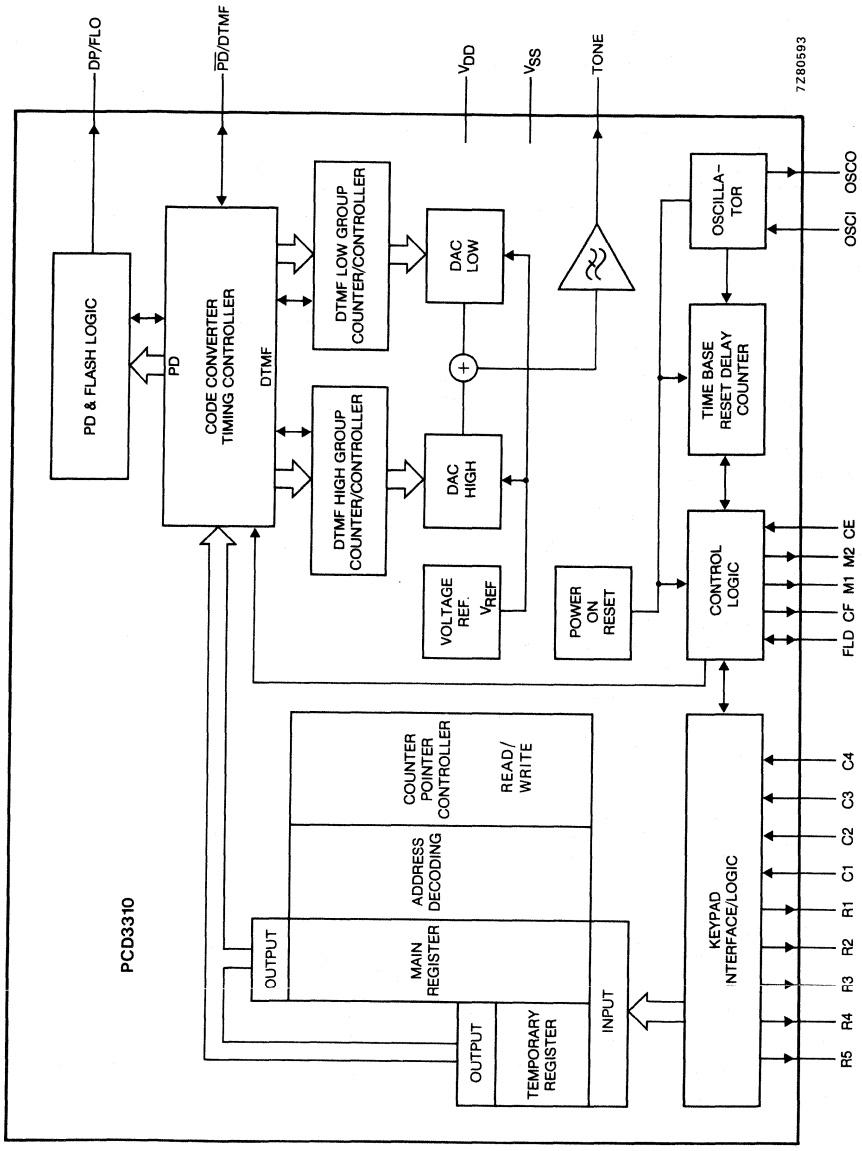


Fig. 1 Block diagram.

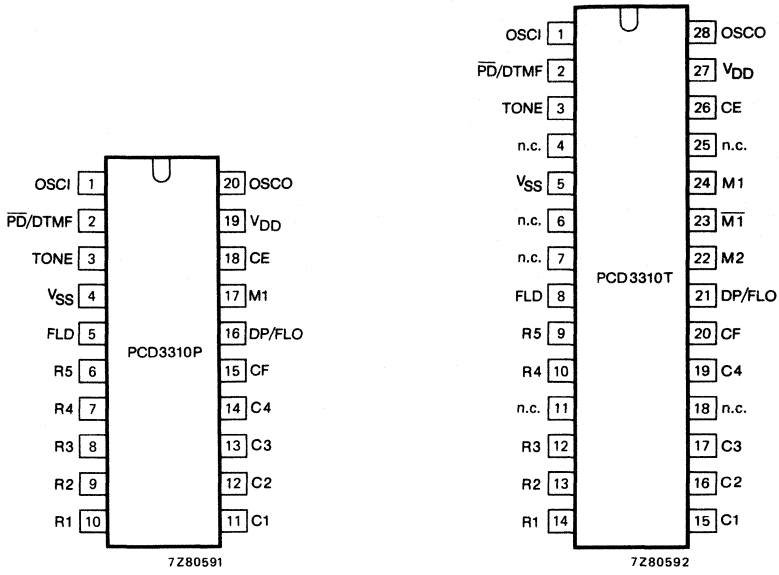


Fig. 2 Pinning diagrams.

DTMF/MODEM/MUSICAL-TONE GENERATORS

GENERAL DESCRIPTION

The PCD3311 and PCD3312 are single-chip silicon gate CMOS integrated circuits. They are intended to provide dual-tone multi-frequency (DTMF) combinations required for tone dialling systems in telephone sets which contain a microcontroller for the control functions.

The various audio output frequencies are generated from an on-chip 3,58 MHz quartz crystal-controlled oscillator.

The devices can interface directly to all standard microcontrollers by accepting a binary-coded parallel input or serial data input (I^2C bus).

With their on-chip voltage reference the PCD3311 and PCD3312 provide constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with the CEPT CS 203 recommendations.

In addition to the standard DTMF frequencies the devices provide 12 MODEM frequencies (300 to 1200 bits per second) used in simplex MODEM applications and two octaves of musical scale in steps of semitones.

Features

- Stabilized output voltage level
- Low output distortion with on-chip filtering (CEPT CS 203 compatible)
- Latched inputs for data bus applications
- I^2C bus compatible
- Mode select input (selection of parallel or serial data input)
- MODEM and melody tone generators

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current	I_{DD}	–	–	1,2	mA
Static standby current	I_{DDO}	–	–	3	μA
DTMF output voltage level (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion	THD	–	−25	–	dB
Operating ambient temperature range	T_{amb}	−25	–	+70	°C

PACKAGE OUTLINES

PCD3311P: 14-lead DIL; plastic (SOT-27K, M, T).
PCD3311T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).
PCD3312P: 8-lead DIL; plastic (SOT-97A).
PCD3312T: 8-lead mini-pack; plastic (VSO-8; SOT-176).

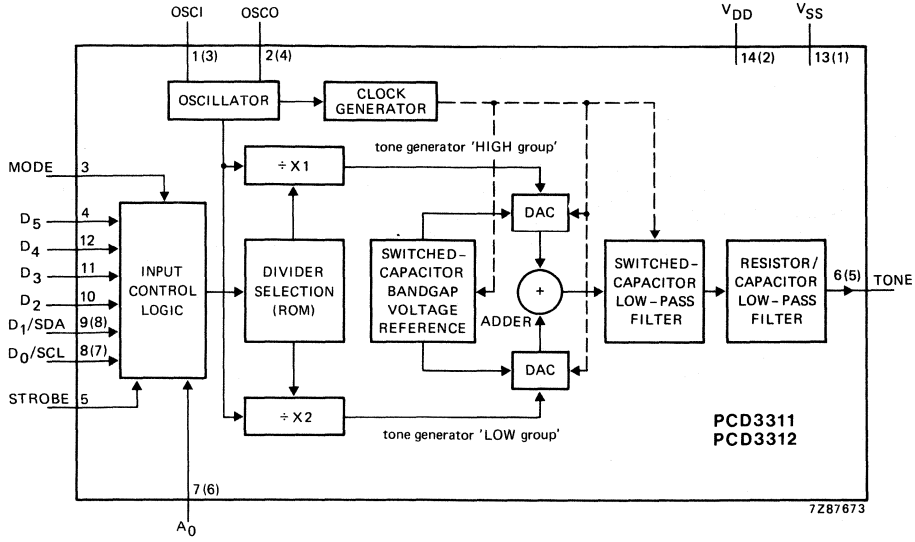


Fig. 1 Block diagram; the pin numbers in parenthesis refer to the PCD3312.

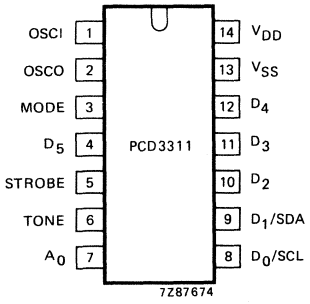


Fig. 2 Pinning diagram for the PCD3311.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D_5	parallel data input*
5	STROBE	strobe input; used for the loading of data in the parallel mode
6	TONE	frequency output for single or dual tones
7	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
8	D_0/SCL	parallel data input* or serial clock line (I^2C bus)
9	D_0/SDA	parallel data input* or serial data line (I^2C) bus)
10	D_2	parallel data inputs*
11	D_3	
12	D_4	
13	V_{SS}	negative supply
14	V_{DD}	positive supply

* MODE = HIGH.

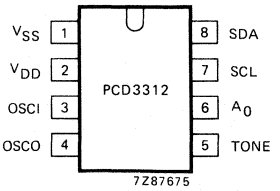


Fig. 3 Pinning diagram for the PCD3312.

PINNING

1	V_{SS}	negative supply
2	V_{DD}	positive supply
3	OSCI	oscillator input
4	OSCO	oscillator output
5	TONE	frequency output for single or dual tones
6	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
7	SCL	serial clock line (I^2C bus)
8	SDA	serial data line (I^2C bus)

FUNCTIONAL DESCRIPTION

Clock/oscillator (OSCI and OSCO)

The timebase for the PCD3311 and PCD3312 is a crystal-controlled oscillator with a 3,58 MHz quartz crystal connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock.

Mode select (MODE)

This input selects the data input mode. When connected to V_{DD}, data can be received in the parallel mode (only for the PCD3311), or, when connected to V_{SS} or left open, data can be received via the serial I^2C bus (for both PCD3311 and PCD3312).

Parallel mode can only be obtained for the PCD3311 by setting MODE input HIGH.

Data inputs (D_0, D_1, D_2, D_3, D_4 and D_5)

Inputs D_0 and D_1 have no internal pull-down or pull-up resistors and must not be left open in any application. Inputs D_2 to D_5 have internal pull-down. D_5 and D_4 are used to select between DTMF dual, DTMF single, MODEM and melody tones (see Table 1). D_3 to D_0 select the combination of the tones for DTMF or single-tone itself.

Table 1 D_5 and D_4 in accordance with the selected application

D_5	D_4	application
0	0	DTMF single tones; standby; melody tones
0	1	DTMF dual tones (all 16 combinations)
1	0	MODEM tones; standby; melody tones
1	1	melody tones

1 = H = HIGH voltage level
0 = L = LOW voltage level

Note: Tables 2, 3, 4 and 5 show all input codes and their corresponding output frequencies.

FUNCTIONAL DESCRIPTION (continued)

Strobe input (STROBE, only for the PCD3311)

This input (with internal pull-down) allows the loading of parallel data into D_0 to D_5 when MODE is HIGH.

The data inputs must be stable preceeding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received.

Serial mode can only be obtained for the PCD3311 by setting MODE input LOW.

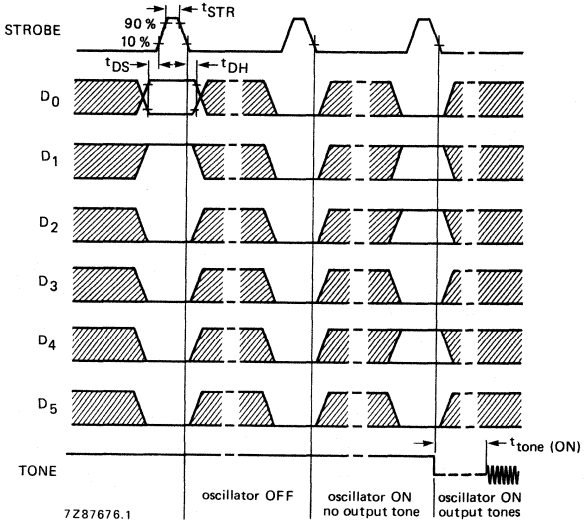


Fig. 4 Timing diagram showing control possibilities of the oscillator and the TONE output (e.g. 770 Hz + 1477 Hz) in the parallel mode (MODE = HIGH).

Serial clock and data inputs (SCL and SDA)

SCL and SDA are combined with D_0 and D_1 respectively. For the PCD3311 the selection of SCL and SDA is controlled by the MODE input. SCL and SDA are serial clock and data lines according to the I^2C bus specification (see "CHARACTERISTICS OF THE I^2C BUS"). Both inputs must be pulled-up externally to V_{DD}.

Address input (A_0)

A_0 is the slave address input and it identifies the device when up to two PCD3311 or PCD3312 devices are connected to the same I^2C bus. In any case A_0 must be connected to V_{DD} or V_{SS}.

I²C bus data configuration (see Fig. 5)

The PCD3311 and PCD3312 are always slave receivers in the I²C bus configuration (R/$\overline{W}$ bit = 0).

The slave address consists of 7 bits in the serial mode for the PCD3311 as well as for the PCD3312, where the least significant bit is selectable by hardware on input A_0 and the other more significant bits are internally fixed. In the serial mode the same input codes are used as in the parallel mode (see Tables 2, 3, 4, and 5). D_6 and D_7 are don't care (X) bits.

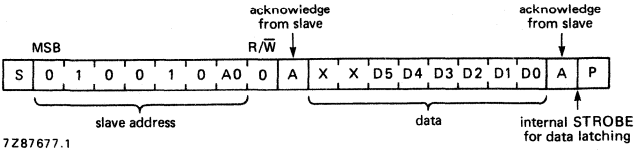


Fig. 5 I²C bus data format.

Tone output (TONE)

The single and the dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 3 shows the frequency tolerance of the output tones for DTMF signalling; Tables 4 and 5 for the modem and melody tones.

Power-on reset

In order to avoid undefined states of the devices when the power is switched ON, an internal reset circuit sets them to the standby mode (oscillator OFF).

Table 2 Input data for control (no output tone; TONE at V_{DD})

D_5	D_4	D_3	D_2	D_1	D_0	HEX	oscillator
X	0	0	0	0	0	00/20	ON
X	0	0	0	0	1	01/21	OFF
X	0	0	0	1	0	02/22	OFF
X	0	0	0	1	1	03/23	OFF

1 = H = HIGH voltage level
0 = L = LOW voltage level
X = don't care

FUNCTIONAL DESCRIPTION (continued)

Table 3 Input data for DTMF

D_5	D_4	D_3	D_2	D_1	D_0	HEX	symbol	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz
0	0	1	0	0	0	08		697	697,90	+ 0,13	+ 0,90
0	0	1	0	0	1	09		770	770,46	+ 0,06	+ 0,46
0	0	1	0	1	0	0A		852	850,45	−0,18	−1,55
0	0	1	0	1	1	0B		941	943,23	+ 0,24	+ 2,23
0	0	1	1	0	0	0C		1209	1206,45	−0,21	−2,55
0	0	1	1	0	1	0D		1336	1341,66	+ 0,42	+ 5,66
0	0	1	1	1	0	0E		1477	1482,21	+ 0,35	+ 5,21
0	0	1	1	1	1	0F		1633	1638,24	+ 0,32	+ 5,24
0	1	0	0	0	0	10	0	941+1336			
0	1	0	0	0	1	11	1	697+1209			
0	1	0	0	1	0	12	2	697+1336			
0	1	0	0	1	1	13	3	697+1477			
0	1	0	1	0	0	14	4	770+1209			
0	1	0	1	0	1	15	5	770+1336			
0	1	0	1	1	0	16	6	770+1477			
0	1	0	1	1	1	17	7	852+1209			
0	1	1	0	0	0	18	8	852+1336			
0	1	1	0	0	1	19	9	852+1477			
0	1	1	0	1	0	1A	A	697+1633			
0	1	1	0	1	1	1B	B	770+1633			
0	1	1	1	0	0	1C	C	852+1633			
0	1	1	1	0	1	1D	D	941+1633			
0	1	1	1	1	0	1E	*	941+1209			
0	1	1	1	1	1	1F	#	941+1477			

Table 4 Input data for MODEM frequencies

D_5	D_4	D_3	D_2	D_1	D_0	HEX	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz	remarks
1	0	0	1	0	0	24	1300	1296,94	−0,24	−3,06	V.23
1	0	0	1	0	1	25	2100	2103,14	+ 0,15	+ 3,14	
1	0	0	1	1	0	26	1200	1197,17	−0,24	−2,83	Bell 202
1	0	0	1	1	1	27	2200	2192,01	−0,36	−7,99	
1	0	1	0	0	0	28	980	978,82	−0,12	−1,18	V.21
1	0	1	0	0	1	29	1180	1179,03	−0,08	−0,97	
1	0	1	0	1	0	2A	1070	1073,33	+ 0,31	+ 3,33	Bell 103
1	0	1	0	1	1	2B	1270	1265,30	−0,37	−4,70	
1	0	1	1	0	0	2C	1650	1655,66	+ 0,34	+ 5,66	V.21
1	0	1	1	0	1	2D	1850	1852,77	+ 0,15	+ 2,77	
1	0	1	1	1	0	2E	2025	2021,20	−0,19	−3,80	Bell 103
1	0	1	1	1	1	2F	2225	2223,32	−0,08	−1,68	

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level
0 = L = LOW voltage level

Table 5 Input data for melody tones

D_5	D_4	D_3	D_2	D_1	D_0	HEX	note	standard frequency Hz*	tone output frequency Hz**
1	1	0	0	0	0	30	D#5	622,3	622,5
1	1	0	0	0	1	31	E5	659,3	659,5
1	1	0	0	1	0	32	F5	698,5	697,9
1	1	0	0	1	1	33	F#5	740,0	741,1
1	1	0	1	0	0	34	G5	784,0	782,1
1	1	0	1	0	1	35	G#5	830,6	832,3
1	1	0	1	1	0	36	A5	880,0	879,3
1	1	0	1	1	1	37	A#5	932,3	931,9
1	1	1	0	0	0	38	B5	987,8	985,0
1	1	1	0	0	1	39	C6	1046,5	1044,5
1	1	1	0	1	0	3A	C#6	1108,7	1111,7
1	0	1	0	0	1	29	D6	1174,7	1179,0
1	1	1	0	1	1	3B	D#6	1244,5	1245,1
1	1	1	1	0	0	3C	E6	1318,5	1318,9
1	1	1	1	0	1	3D	F6	1396,9	1402,1
0	0	1	1	1	0	0E	F#6	1480,0	1482,2
1	1	1	1	1	0	3E	G6	1568,0	1572,0
1	0	1	1	0	0	2C	G#6	1661,2	1655,7
1	1	1	1	1	1	3F	A6	1760,0	1768,5
0	0	0	1	0	0	04	A#6	1864,7	1875,1
0	0	0	1	0	1	05	B6	1975,5	1970,0
1	0	0	1	0	1	25	C7	2093,0	2103,1
1	0	1	1	1	1	2F	C#7	2217,5	2223,3
0	0	0	1	1	0	06	D7	2349,3	2358,1
0	0	0	1	1	1	07	D#7	2489,0	2470,4

* Standard scale based on A4 = 440 Hz.

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level

0 = L = LOW voltage level

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

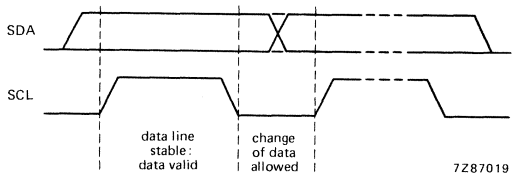


Fig. 6 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

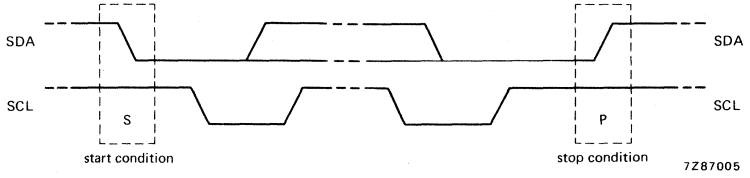


Fig. 7 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

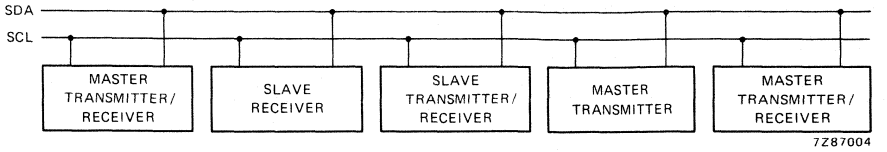


Fig. 8 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

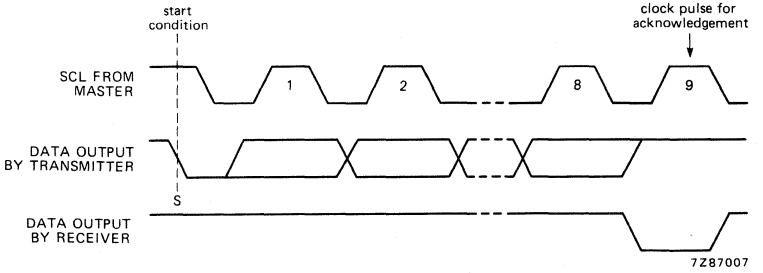


Fig. 9 Acknowledgement on the I^2C bus.

CHARACTERISTICS OF THE I²C BUS (continued)

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The ICs operate in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

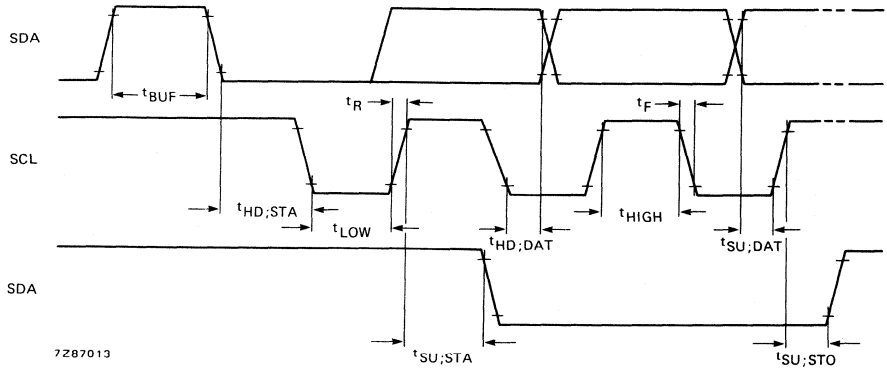


Fig. 10 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

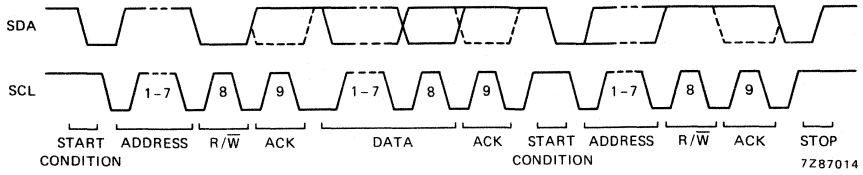


Fig. 11 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 12.

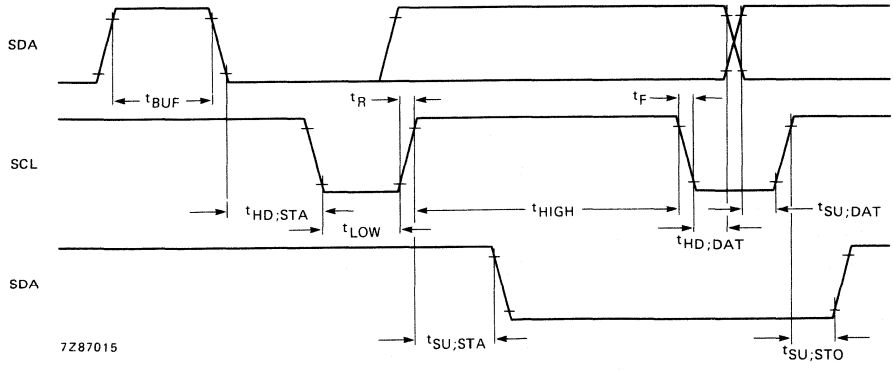


Fig. 12 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

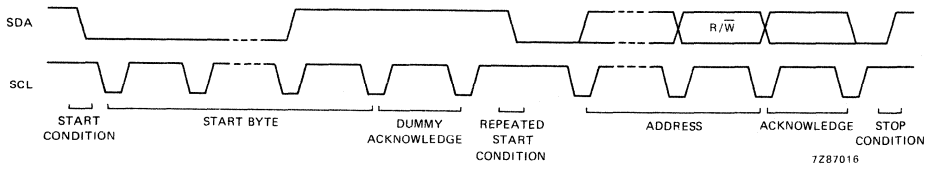


Fig. 13 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,8	+ 8,0	V
Input voltage range (any input)	V_I	−0,8	V_{DD}+0,8	V
D.C. input current (any input)	$\pm I_I$	—	10	mA
D.C. output current (any output)	$\pm I_O$	—	10	mA
Supply current	$\pm I_{DD}$; $\pm I_{SS}$	—	50	mA
Power dissipation per output	P_O	—	50	mW
Total power dissipation per package	P_{tot}	—	300	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579 545 MHz, R_{Smax} = 50 Ω; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	—	6,0	V
Operating supply current (note 1) oscillator ON; V_{DD} = 3 V					
no output tone	I_{DD}	—	50	100	μA
single output tone	I_{DD}	—	0,5	1,0	mA
dual output tone	I_{DD}	—	0,6	1,2	mA
Static standby current oscillator OFF; note 1	I_{DDO}	—	—	3	μA
Inputs/outputs (SDA)					
D_0 to D_5; MODE; STROBE					
Input voltage LOW	V_{IL}	0	—	0,3 x V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	—	V_{DD}	V
D_2 to D_5; MODE; STROBE; A_0					
Pull-down input current V_I = V_{DD}	$-I_{IL}$	30	150	300	nA
SCL (D_0); SDA (D_1)					
Output current LOW (SDA) V_{OL} = 0,4 V	I_{OL}	3	—	—	mA
Clock frequency (see Fig. 10)	f_{SCL}	—	—	100	kHz
Input capacitance; V_I = V_{SS}	C_I	—	—	7	pF
Allowable input spike pulse width	t_I	—	—	100	ns

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 14)					
DTMF output voltage levels (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
D.C. voltage level	V_{DC}	–	½ V_{DD}	–	V
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion T_{amb} = 25 °C					
dual tone; note 2	THD	–	–25	–	dB
modem tone, note 3	THD	–	–29	–	dB
Output impedance	$\|Z_O\|$	–	0,1	0,5	kΩ
OSCI input					
Maximum allowable amplitude at OSCI	$V_{OSC(p-p)}$	–	–	$V_{DD}-V_{SS}$	V
Timing (V_{DD} = 3 V)					
Oscillator start-up time	$t_{OSC(ON)}$	–	3	–	ms
TONE start-up time; note 4	$t_{TONE(ON)}$	–	0,5	–	ms
STROBE pulse width; note 5	t_{STR}	400	–	–	ns
Data set-up time; note 5	t_{DS}	150	–	–	ns
Data hold time; note 5	t_{DH}	100	–	–	ns

Notes to the characteristics

1. Crystal is connected between OSCI and OSCO; D_0/SCL and D_1/SDA via a resistance of 5,6 kΩ to V_{DD}; all other pins left open.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Related to the level of the fundamental frequency.
4. Oscillator must be running.
5. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

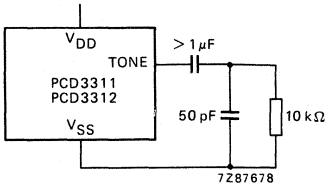


Fig. 14 TONE output test circuit.

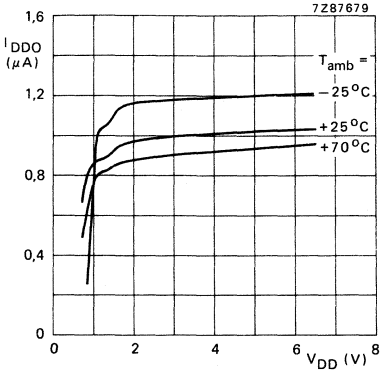


Fig. 15 Standby supply current as a function of supply voltage; oscillator OFF.

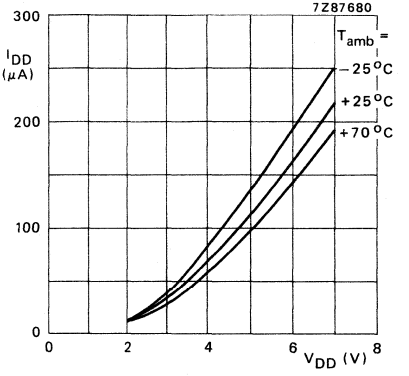


Fig. 16 Operating supply current as a function of supply voltage; oscillator ON; no output at TONE.

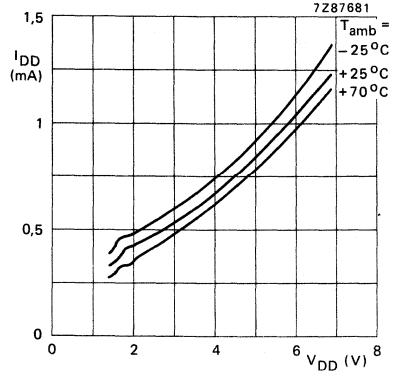


Fig. 17 Operating supply current as a function of supply voltage; oscillator ON; dual tone at TONE.

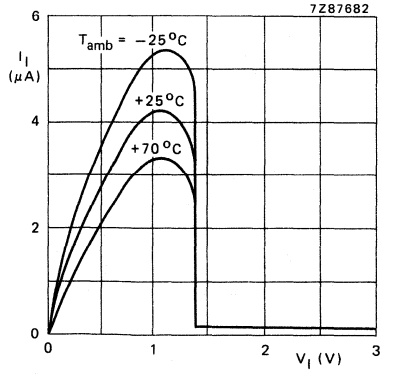


Fig. 18 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

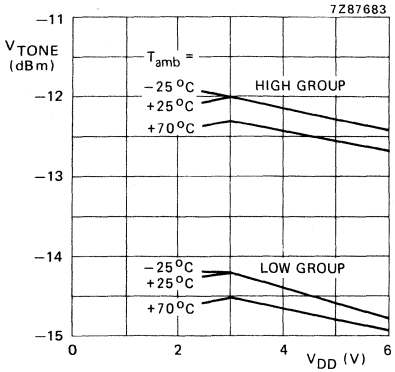


Fig. 19 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

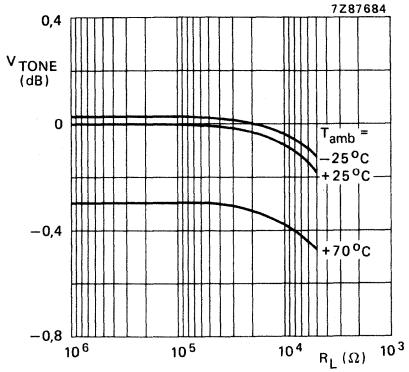


Fig. 20 Dual tone output voltage level as a function of output load resistance.

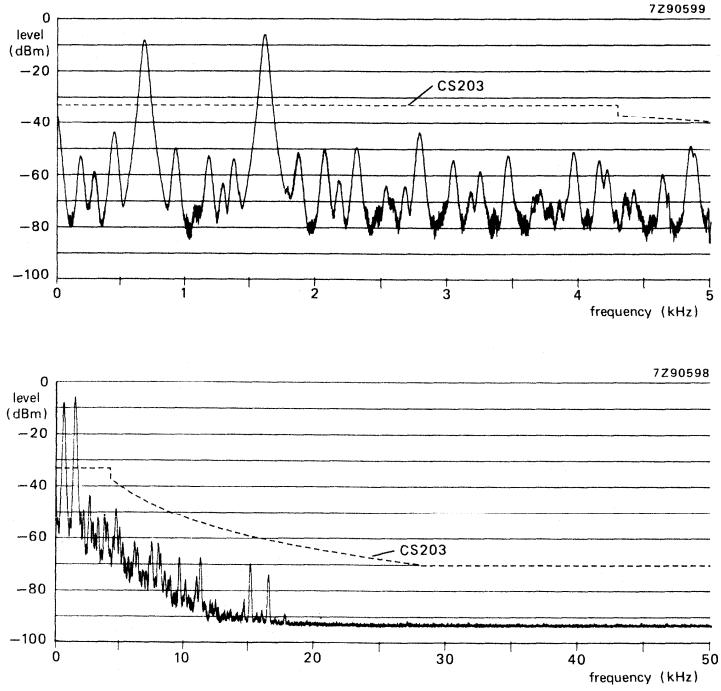


Fig. 21 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

APPLICATION INFORMATION

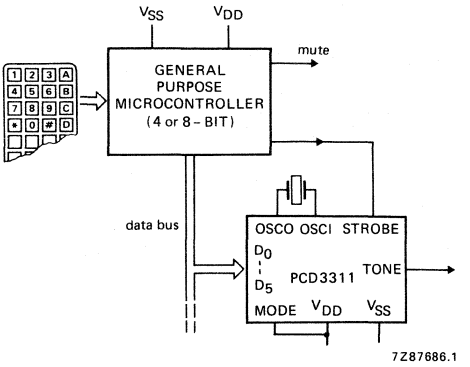


Fig. 22 PCD3311 driven by a microcontroller with parallel data-bus.

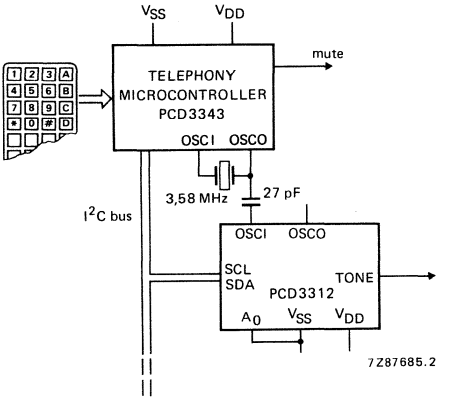


Fig. 23 PCD3312 driven by telephony microcontroller PCD3343 with serial I/O (I^2C bus).
The PCD3343 is a single-chip 8-bit microcontroller with 3K ROM/224 RAM bytes. The same application is possible with the PCD3311 with MODE = V_{SS}.

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

CMOS REDIAL AND REPERTORY DIALLER

GENERAL DESCRIPTION

The PCD3315 is a single chip CMOS dialler IC for telephone sets. It has two dialling modes; pulse dialling (PD), and dual tone multi-frequency (DTMF) when used in conjunction with tone generator PCD3312. As well as manual dialling it also features several automatic functions, e.g. redial, extended redial, notepad and repertory dial.

Features

- Pulse dialling
- DTMF dial control of tone generator PCD3312
- Redial
- Extended redial
- Electronic notepad
- Ten repertory dial numbers
- 18-digit capacity for each autodial memory
- Maximum of 36 digits per call
- Flash or register recall
- Uses standard 4x4 keyboard (single or double contact)
- Four extra function keys: program/autodial, flash, redial, access pause
- Access pause generation and termination
- Automatic PABX-digit recognition; resulting in an access pause insertion
- Hold input and access pause output (APO) to adjust the duration of the access pause and facilitate use of tone recognisers
- Four diode or strap functions: general/German, access pause time, reset delay time, general: mark-space ratio/German: prepulse
- Manual reset of autodial RAM
- On-chip power-on reset
- Programmed for improved noise immunity

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,75 to 6,0	V
Standby supply voltage	V_{DD}	min. 1	V
Operating currents at V_{DD} = 3 V, conversation mode	I_{DD}	typ. 300	μA
Standby supply current at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DD}	typ. 1,2	μA
Crystal frequency	f	3,58	MHz
Operating ambient temperature range	T_{amb}	−25 to +70	°C

PACKAGE OUTLINES

PCD3315P: 28-lead DIL; plastic (SOT-117).
PCD3315T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

PINNING

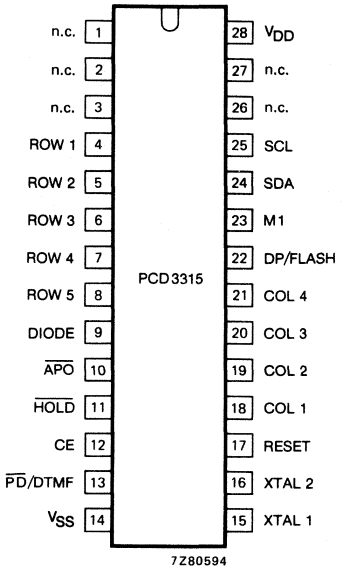


Fig. 1 Pinning diagram.

TIMING DATA, GENERAL VERSION *

Reset delay time *	t_{rds}		160 or 320 ms
Reset delay time during access pause	t_{rds}		320 ms
Keyboard debounce time	t_{db}		20 ms
Flash time	t_{fl}		95 ms
Pulse dialling			
Dial frequency	f_d		10 Hz
Break/make time *	$t_{b/m}$		60,40 or 67,33 ms
Interdigit pause	t_{idp}		840 ms
Access pause *	t_{ap}		3 or 5 s
Mute hold-over time (only during access pause)	t_h		1 s
DTMF dialling			
Tone transmission time	t_t	min.	70 ms or key-down time
Tone pause time	t_p	min.	70 ms
Mute hold-over time during dialling	t_h		80 ms
Mute hold-over time during access pause	t_h		1 s
Access pause *	t_{ap}		1,5 or 2,5 s

* Value is determined by diode option.

TIMING DATA, GERMAN VERSION *

Reset delay time *	t_{rds}	160 or 320	ms
Reset delay time during access pause	t_{rds}	320	ms
Keyboard debounce time	t_{db}	20	ms

Pulse dialling

Dial frequency	f_d	10	Hz
Break/make times	$t_{b/m}$	60, 40	ms
Interdigit pause	t_{idp}	840	ms
Access pause *	t_{ap}	3 or 5	s
Mute hold-over time * (only during access pause)	t_h	1 or 3	s
Prepulse time * (if selected)	t_{pp}	20	ms

DTMF dialling

Tone transmission time	t_t	min. 80 ms or key-down time	
Tone pause time	t_p	min. 80	ms
Mute hold-over time during dialling	t_h	80	ms
Mute hold-over time during access pause	t_h	1	s
Access pause *	t_{ap}	1,5 or 2,5	s
Flash time	t_f	95	ms

DEVELOPMENT SAMPLE DATA

* Value is determined by diode option.

KEY PROCEDURE

column	1	2	3	4
row				
1	1	2	3	A
2	4	5	6	B
3	7	8	9	C
4	*	0	#	D
5	P	FL	R	AP

Fig. 2 Keyboard.

Table 1 Key procedure

mode	operation	program
redial	R	automatic
extended redial	P . R	TN . P
notepad	P . R	dial . P . P . TN . P
repertory dial	P . d	$\overline{P}$. d . TN
PABX digitis	automatic	$\overline{P}$. R . d_1 (d_2) R d_3 (d_4)
autodial RAM reset	hook-on: $\overline{2,5,8,0}$	
	hook-off: 2,5,8,0	

Where : P = press and release P-key

$\overline{P}$ = press and keep P-key pressed

R = press and release R-key

TN = telephone number

d = digit 0 to 9

$\overline{2,5,8,0}$ = press and keep pressed keys 2, 5, 8 and 0

2,5,8,0 = release keys 2, 5, 8 and 0

APPLICATION INFORMATION

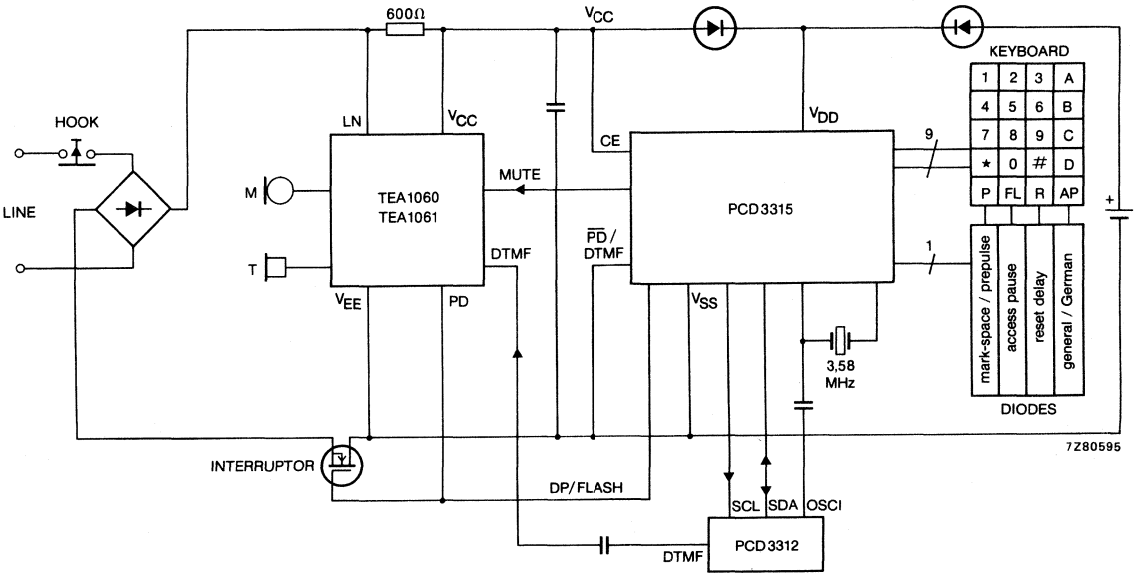


Fig. 3 Simplified application diagram.

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3320 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- All inputs with pull-up/pull-down (except CE).
- 23-digit capacity for redial operation.
- Circuit reset for line power breaks; $>$ 160 ms.
- Dialling pulse frequency: 10 Hz.
- Test pulse frequency: 932 Hz.
- Hold facility for lengthening the inter-digit period.
- Memory overflow possibility (with internally disabled redial).
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINES

PCD3320P : 18-lead DIL; plastic (SOT-102G).
PCD3320D: 18-lead DIL; ceramic (SOT-133).

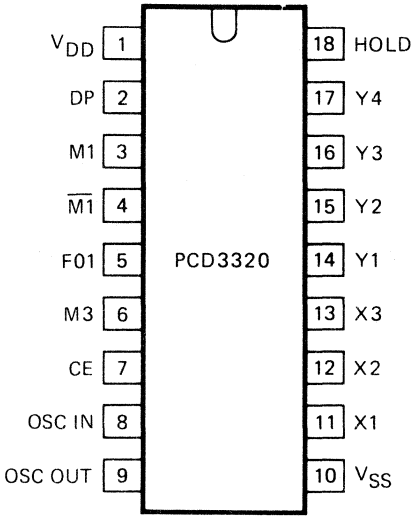


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

5	F01	the dialling pulse frequency is defined by the logic state of this input
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks.
11	X1	column keyboard inputs with pull-down on chip
12	X2	
13	X3	
14	Y1	row keyboard inputs with pull-up on chip
15	Y2	
16	Y3	
17	Y4	
18	HOLD	interrupts dialling after completion of the current digit or immediately following an inter-digit pause (t_{id}); further keyboard data will be accepted

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	M1	Muting; normally used for muting during the dialling sequence
4	$\overline{M1}$	inverted output of M1
6	M3	AND function, with $\overline{DP}$ and M1 as input, for direct drive of a switching transistor for dialling pulses and muting.

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

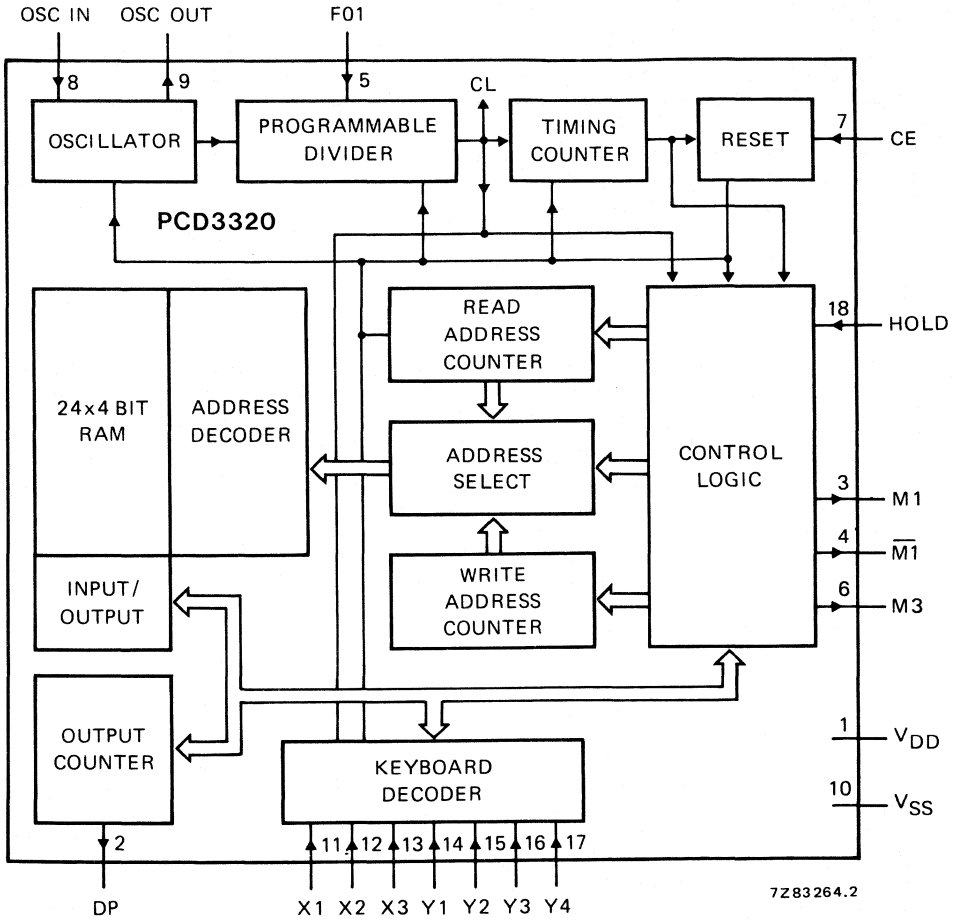


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the PCD3320 is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set by input F01 to provide one of two chip system clocks; the 'normal' clock frequency (F01 = LOW) and the test frequency (F01 = HIGH).

Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

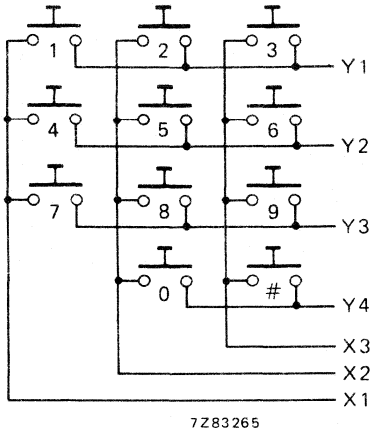
Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored in the RAM and converted into correctly timed dialling pulses.



Redial.

Fig. 3 Single contact keyboard.

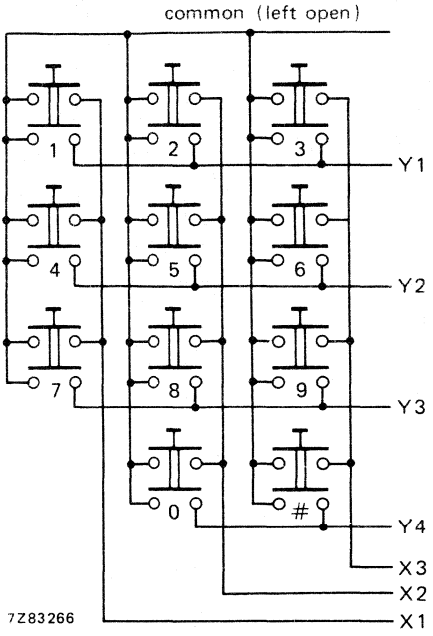


Fig. 4 Double contact keyboard.

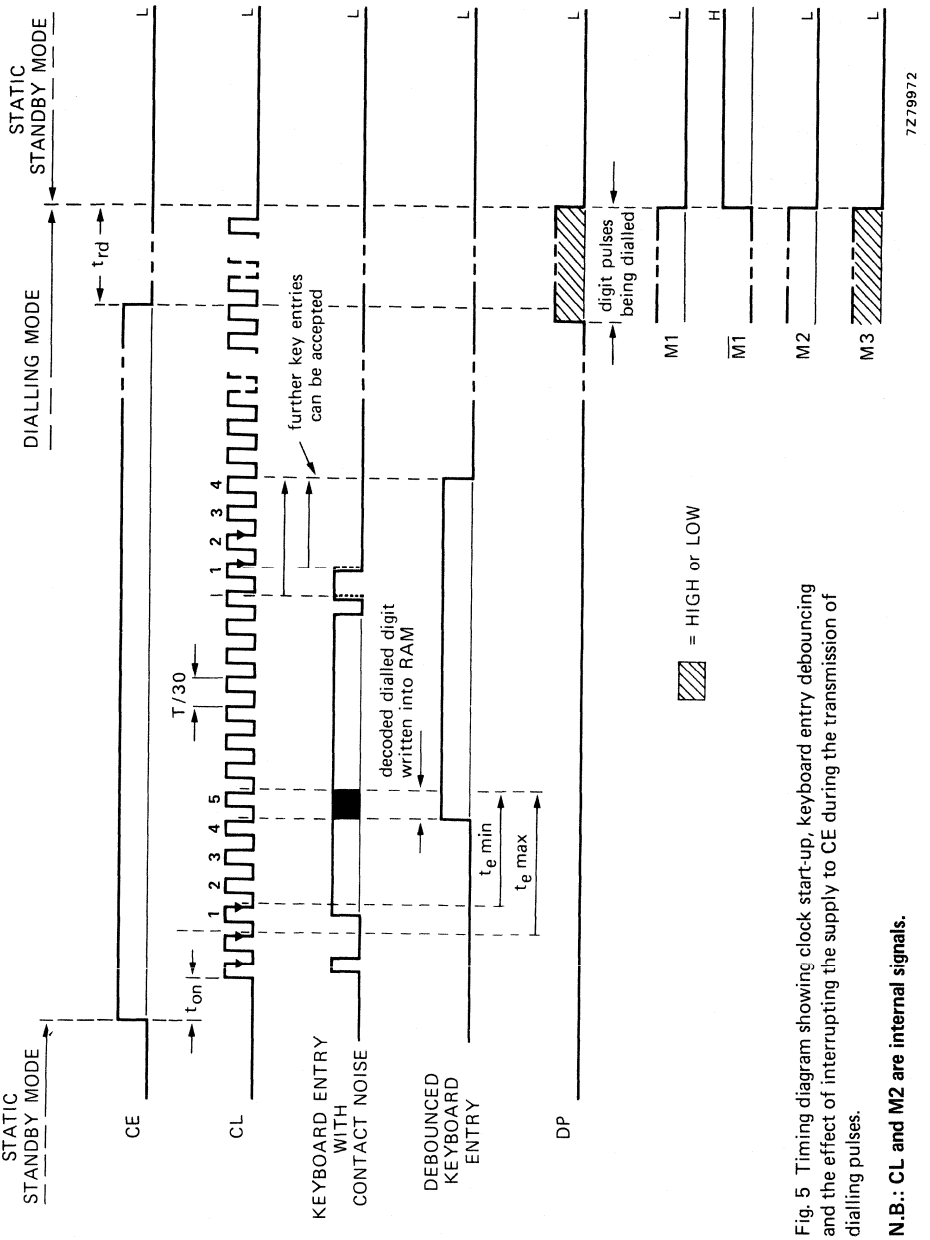


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

N.B.: CL and M2 are internal signals.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at outputs M1 and M3. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at outputs DP and M3. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

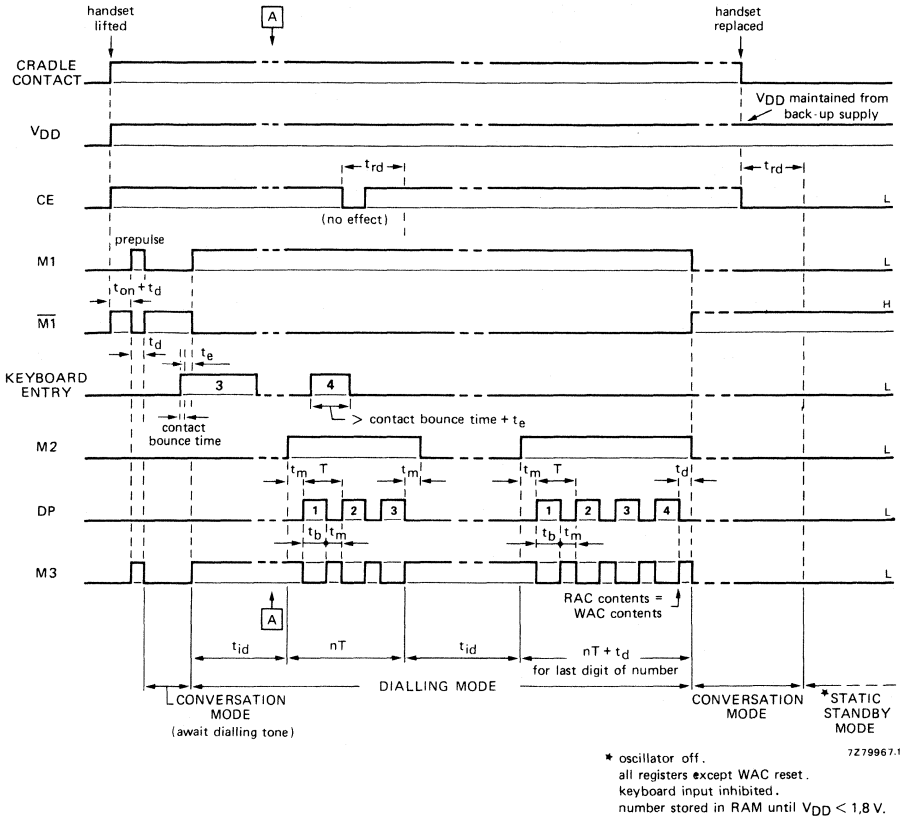


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.

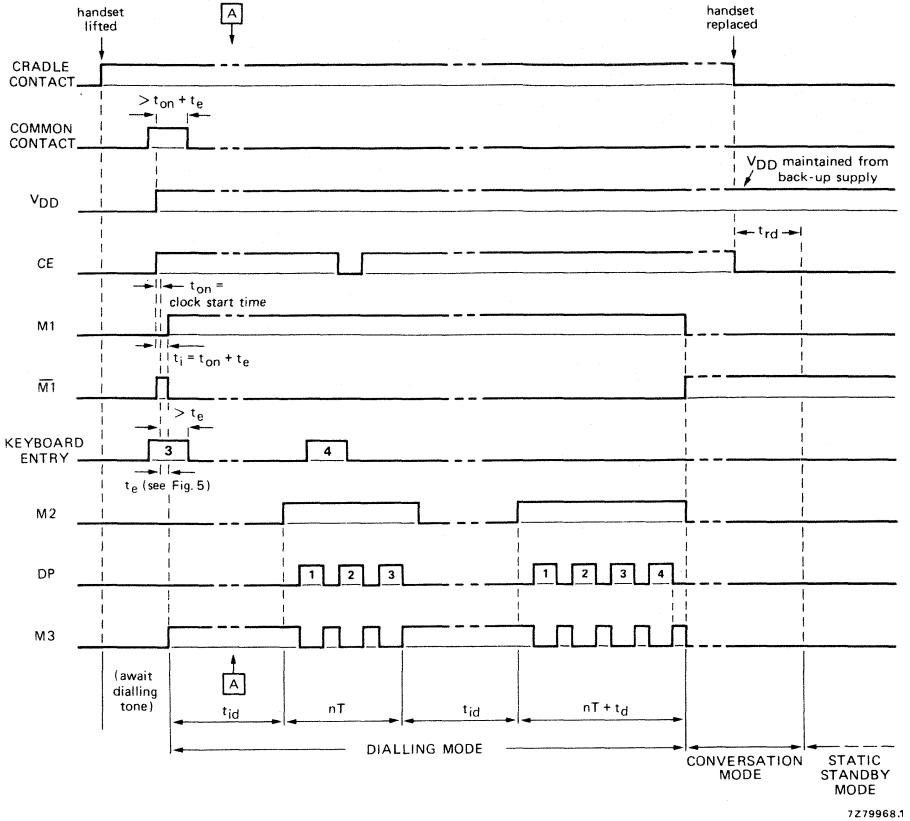


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A. M2 is an internal signal.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD input is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on M3 and DP until the HOLD input is set LOW again and an inter-digit pause has elapsed.

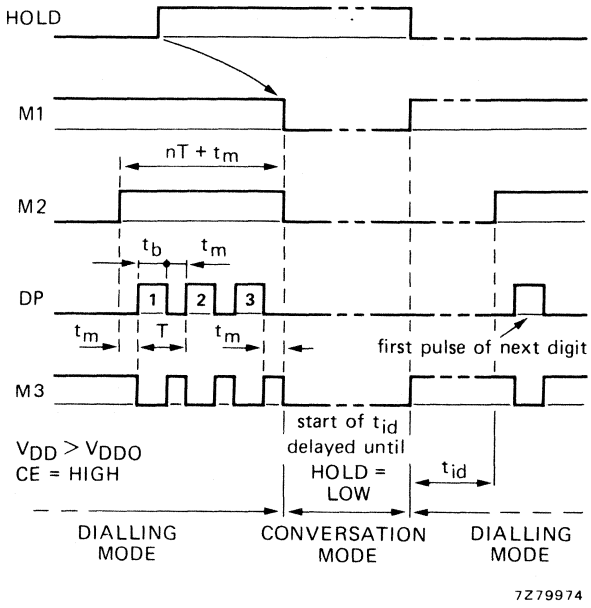


Fig. 8 Timing diagram showing the effect of activating the HOLD input during the transmission of dialling pulses. M2 is an internal signal.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS}−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	T_{amb} = −25 to + 70 °C
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to + 70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = HIGH; notes 2, 3
	I_{DD}	–	50	100	μA	CE = HIGH; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	5	μA	CE = LOW; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V; T_{amb} = −25 to + 70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		1,8 V ⩽ V_{DD} ⩽ 6 V
Input leakage current; CE LOW	$-I_{IL}$	–	–	50	nA	CE = LOW
HIGH	I_{IH}	–	–	50	nA	CE = HIGH
Pull-down input current F01, HOLD	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	V_I = V_{SS}
Output sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
Output source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 8 and 9 < 3 pF.
4. Guarantees correct keyboard operation.

TIMING DATA I

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz; R_{Smax} = 100 Ω

	symbol	min.	typ.	max.		conditions
Clock start-up time	t_{on}	–	4	–	ms	Figs 6, 7; note 1
Initial data entry time ($t_i = t_{on} + t_e$)	$t_{i\,min}$	–	18	–	ms	F01 = LOW } Fig. 7
	$t_{i\,max}$	–	4	–	ms	F01 = HIGH } Fig. 7

TIMING DATA II (exact values)

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,58 MHz

	symbol	F01 = LOW (dialling)	F01 = HIGH (testing)		conditions
Dialling pulse frequency	f_{DP}	10,13	932,2	Hz	note 2
Dialling pulse period; $1/f_{DP}$	T_{DP}	98,7	1,073	ms	Figs 6, 7
Prepulse duration; 1/3 x T_{DP}	t_d	33	0,358	ms	Figs 6, 7
Inter-digit pause; 8 x T_{DP}	t_{id}	790	8,58	ms	Figs 6, 7
Break time; 3/5 x T_{DP}	t_b	59,2	0,644	ms	Fig. 6
Make time; 2/5 x T_{DP}	t_m	39,5	0,429	ms	Fig. 6
Debounce time					
min. 4/30 x T_{DP}	$t_{e\,min}$	13,2	0,143	ms	Fig. 5
max.; 1/6 x T_{DP}	$t_{e\,max}$	16,5	0,179	ms	Fig. 5
Reset delay time; 1,6 x T_{DP}	t_{rd}	158	1,7	ms	Figs 5, 6, 7

Notes

1. Stray capacitance between pins 8 and 9 < 3 pF.
2. Exactly 10 Hz and 920 Hz respectively when a 3,5328 MHz crystal is used.

TYPICAL CURVES

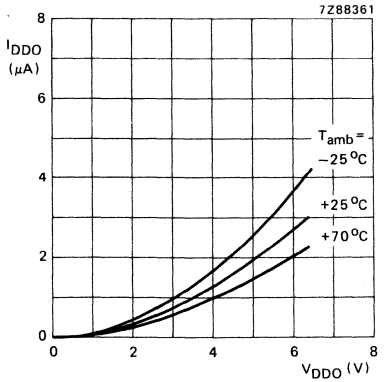


Fig. 9 Standby supply current as a function of standby supply voltage.

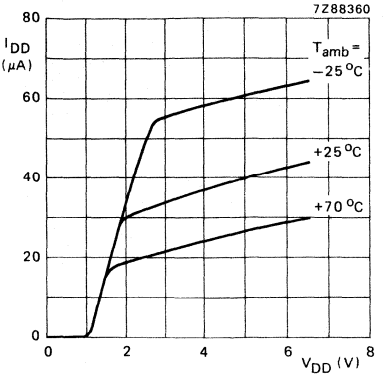


Fig. 10 Operating supply current as a function of operating supply voltage.

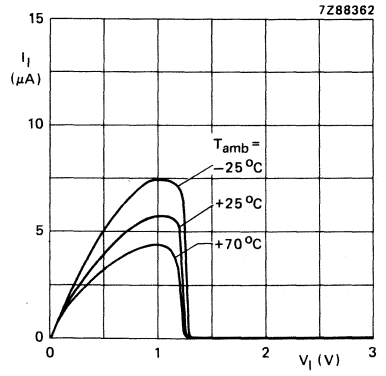


Fig. 11 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

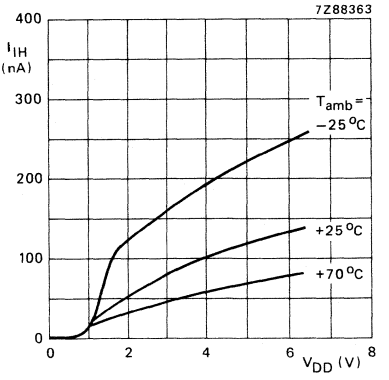


Fig. 12 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

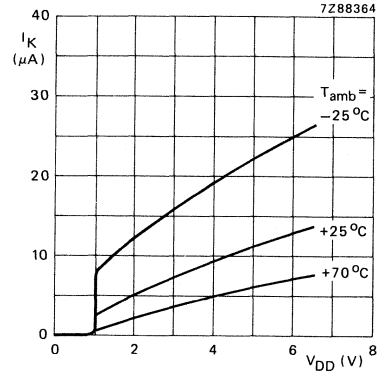


Fig. 13 Keyboard current as a function of supply voltage; X-pins connected to Y-pins.

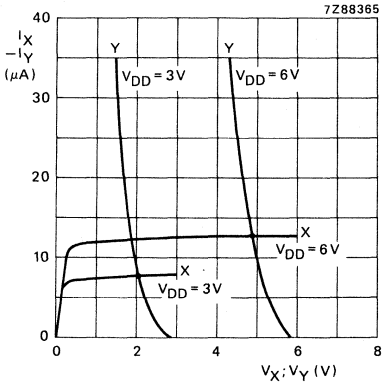


Fig. 14 Keyboard input characteristics at T_{amb} = 25 °C.

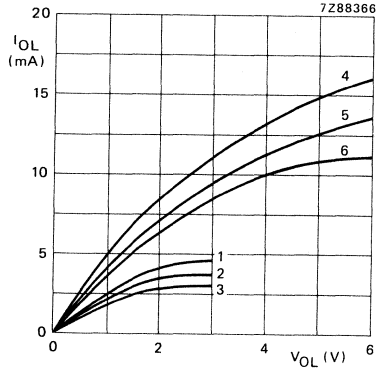


Fig. 15 Output (N-channel) sink characteristics for M1, $\overline{M1}$, M3 and DP.

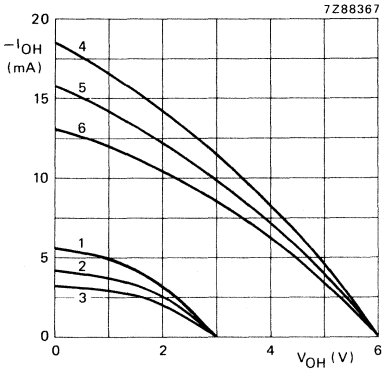


Fig. 16 Output (P-channel) source characteristics for M1, $\overline{M1}$, M3 and DP.

Curves for Figs 15 and 16

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3321 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The PCD3321 can regenerate access pauses during redial. During the original entry, access pauses are stored either automatically or via the keyboard. A regenerated access pause can be terminated during redial in three ways: automatically after a built-in time, or via the keyboard, or with an external dial tone recogniser circuit. This makes the circuit very suitable for redial in PABX (Private Automatic Branch Exchange) systems. The PCD3321 is pin to pin compatible with the DF320 and the MT4320 (however, including additional functions).

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- 23-digit capacity, including access pauses, for redial operation.
- Memory overflow possibility (with internally disabled redial).
- Selectable dialling pulse frequency: 10 Hz, 16 Hz and 20 Hz.
- Test pulse frequency: 932 Hz.
- Selectable dialling pulse mark/space ratios; 2 : 1 or 3 : 2.
- Hold facility for lengthening the inter-digit period.
- Circuit reset for line power breaks; $>$ 160 ms (10 Hz dialling pulse frequency).
- Access pause generation automatically or via the keyboard.
- Access pause reset:
  automatically after 3 s (10 Hz dialling pulse frequency),
  via the keyboard,
  with external tone recogniser.
- All inputs with pull-up/pull-down (except CE).
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINES

PCD3321P: 18-lead DIL; plastic (SOT-102G).
PCD3321D: 18-lead DIL; ceramic (SOT-133).

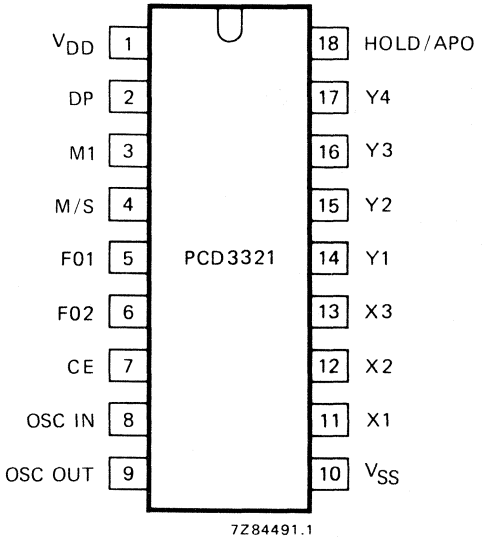


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

4	M/S	controls the mark-to-space ratio of the line pulses
5	F01	the dialling pulse frequency is defined by the logic state of these two inputs
6	F02	
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks
11	X1	column keyboard inputs with pull-down on chip
12	X2	
13	X3	
14	Y1	row keyboard inputs with pull-up on chip
15	Y2	
16	Y3	
17	Y4	

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	M1	Muting; normally used for muting during the dialling sequence

Input/output

18	HOLD/APO	This pin will go HIGH when an access pause code is read from the memory during pulsing and will interrupt dialling. It can also be externally controlled; it will interrupt dialling after completion of the current digit or immediately during an inter-digit pause (t_{id}); further keyboard data will be accepted.

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

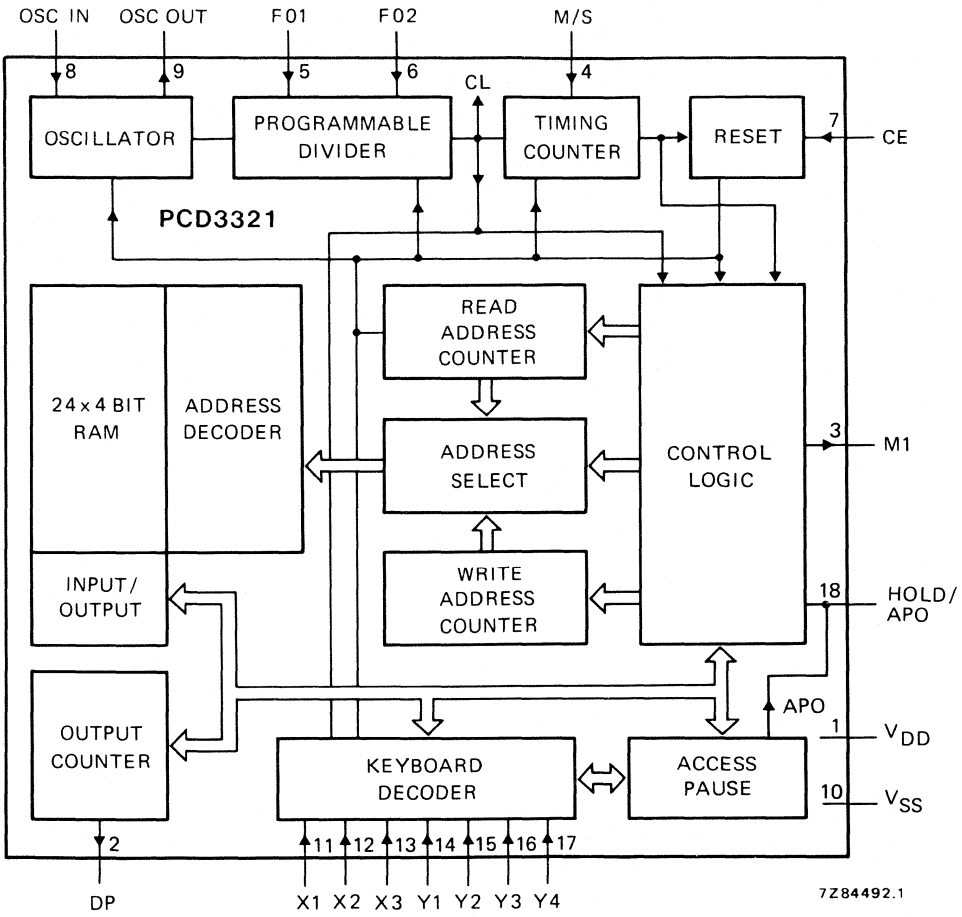


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the PCD3321 is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set (F01 and F02) to provide one of four chip system clocks; three 'normal' clock frequencies and one higher test frequency.

Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

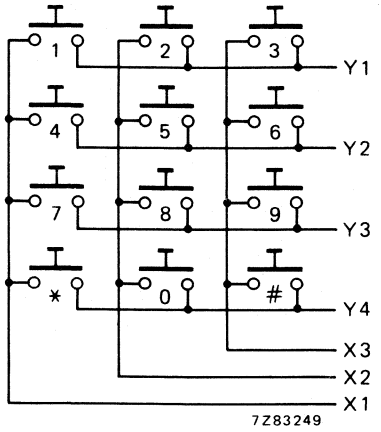
Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the PCD3321. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.



★ Access pause set.

Redial or Access Pause Reset.

Fig. 3 Single contact keyboard.

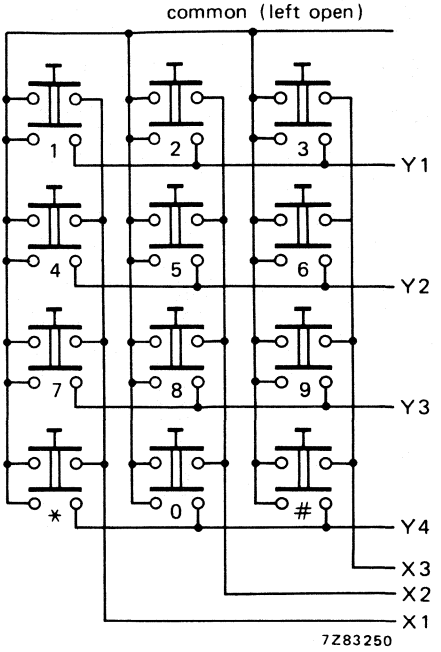


Fig. 4 Double contact keyboard.

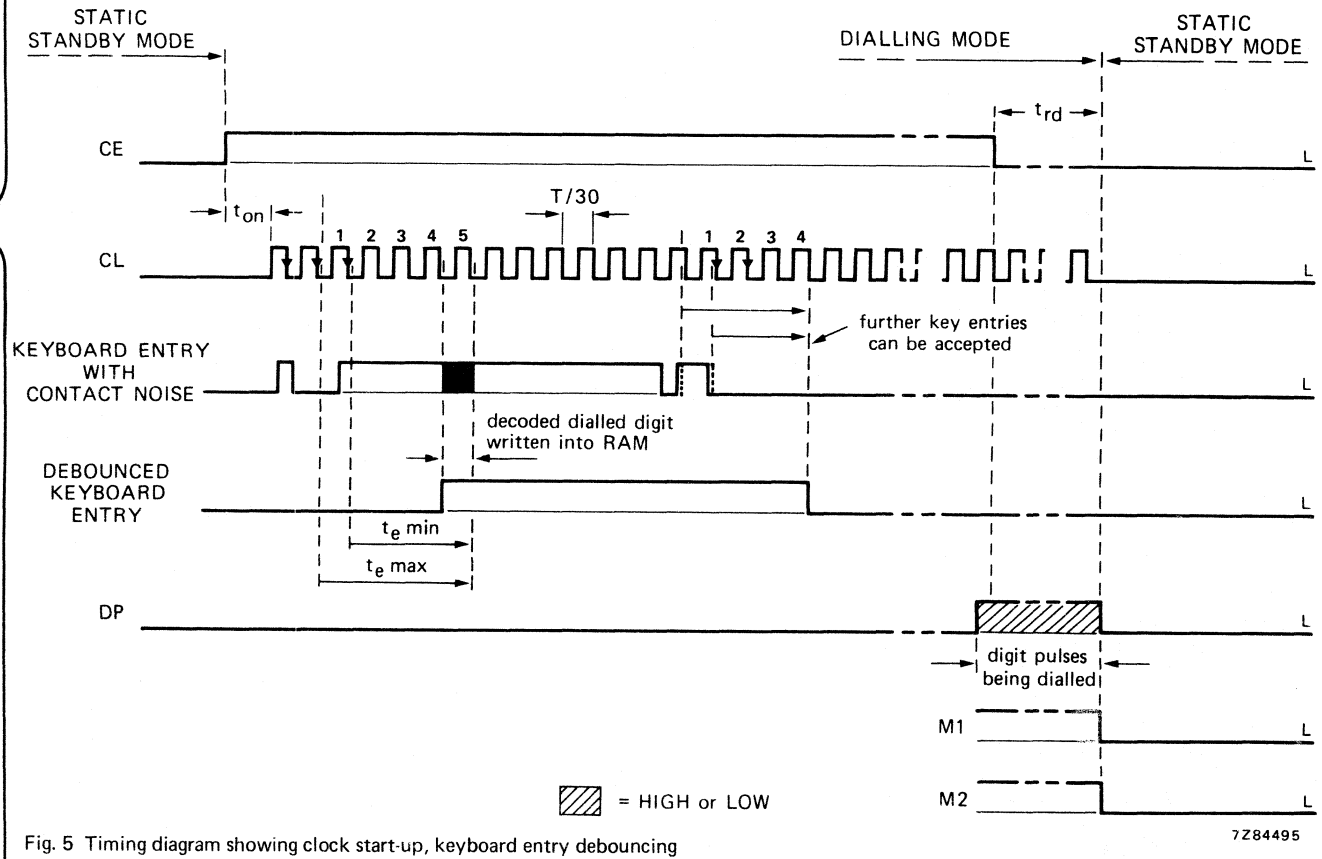


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

N.B.: CL and M2 are internal signals.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at output M1. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

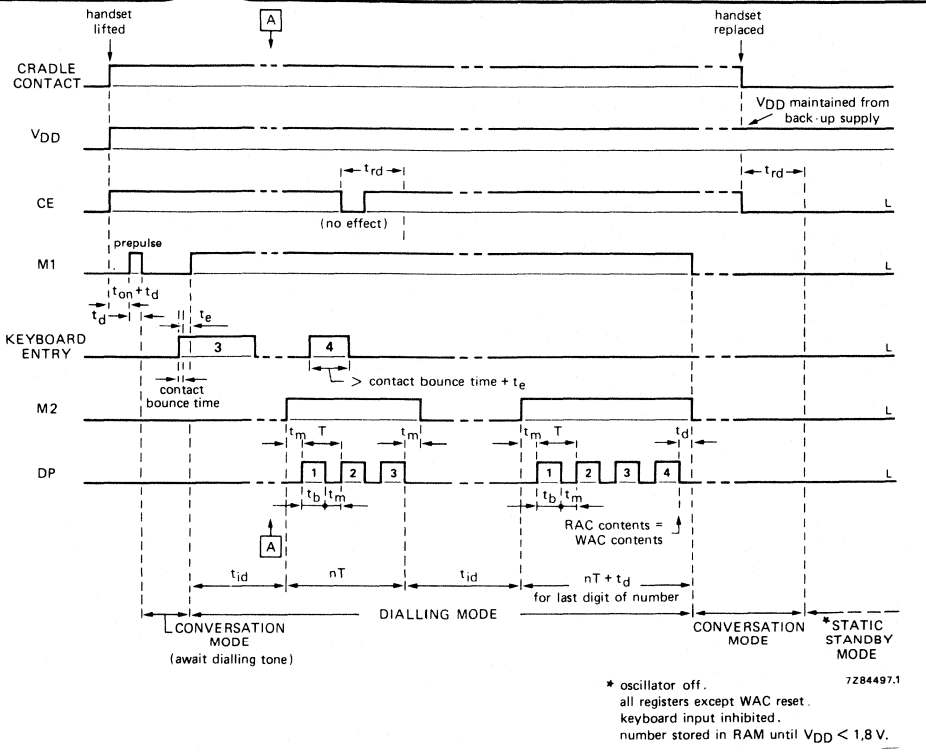


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.

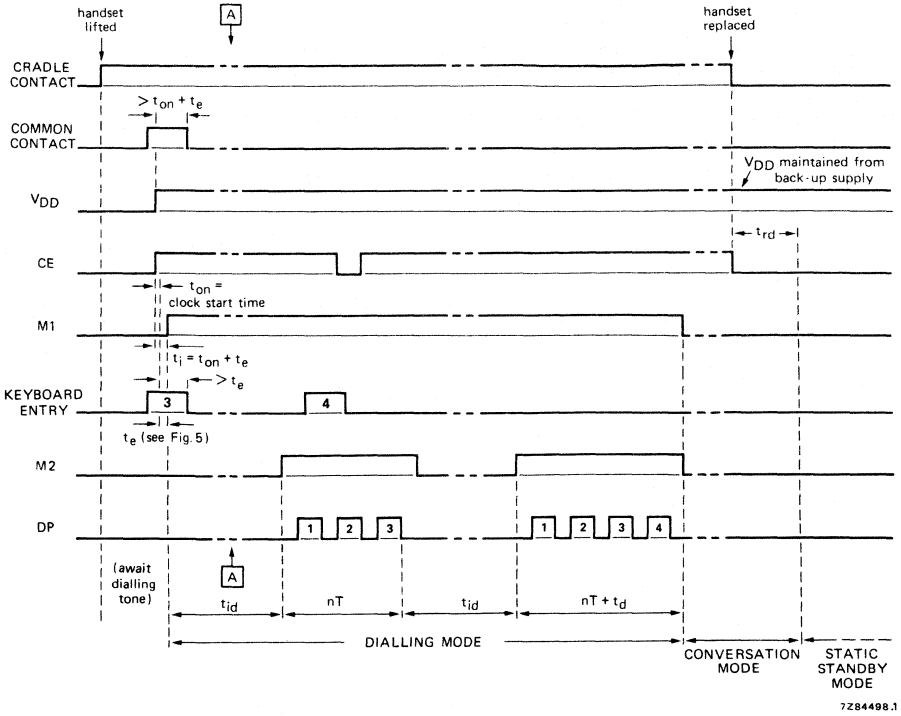


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A. M2 is an internal signal.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD/APO is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on DP until the HOLD/APO is set LOW again and an inter-digit pause has elapsed.

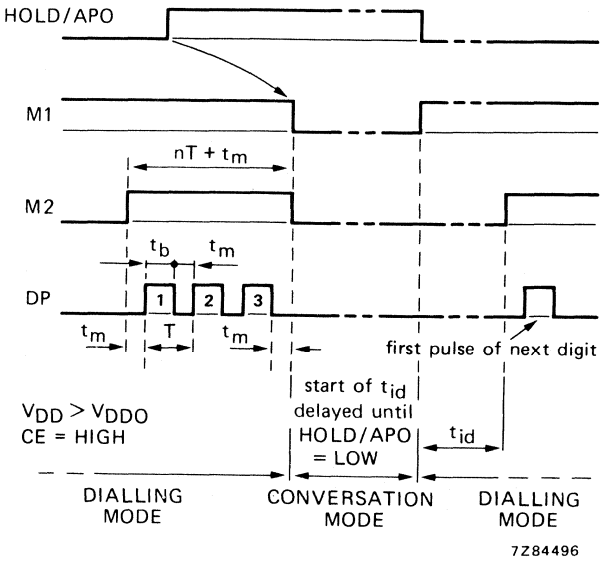


Fig. 8 Timing diagram showing the effect of activating the HOLD/APO during the transmission of dialling pulses. M2 is an internal signal.

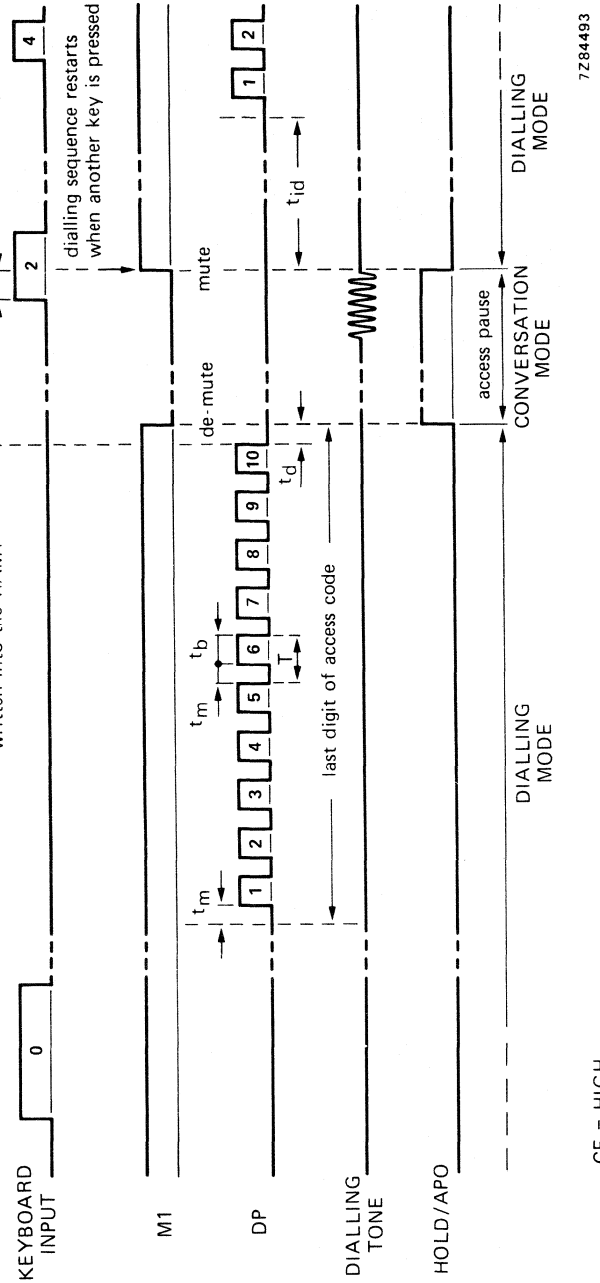
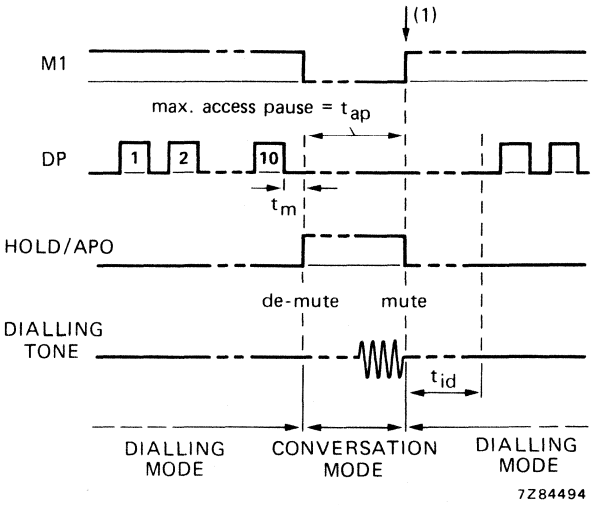


Fig. 9 Dialling sequence showing how an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.

Access pause regeneration during redial

During original entry, access pause codes can be stored at the appropriate positions in the RAM. During redial the Access Pause Output (HOLD/APO)will go HIGH as soon as an access pause code is read from the RAM, thereby interrupting dialling until HOLD/APO is made LOW again as described above. In this way the normal inter-digit pause with a duration t_{id} can be replaced by a proper access pause. An access pause code is now automatically stored in the RAM during original entry, when M1 goes LOW, after all digits so far entered have been transmitted (see Fig. 6). This occurs between entering of the trunk exchange code and the subscriber code, whilst the access tone is available. Up to two access pauses can be entered into the RAM in this manner. Alternatively, the access pause key (★) can still be pressed to insert (more) access pauses manually (digits + access pauses $\leqslant 23$).
During redial, access pauses will be automatically regenerated.

Three methods of terminating an access pause:
1. Automatically, if the built-in time t_{ap} expires; HOLD/APO then goes LOW.
2. Manually, by pressing the redial key before t_{ap} expires.
3. With an external tone recogniser, by forcing HOLD/APO to LOW or HIGH respectively, for shortening or lengthening an access pause.



(1) a. Access pause (t_{ap}) expires or press redial before end of t_{ap}.

b. HOLD/APO controlled by tone recogniser:
HOLD/APO forced to LOW before t_{ap} expires; access pause $< t_{ap}$
HOLD/APO forced to HIGH after t_{ap} expires; access pause $> t_{ap}$.

Fig. 10 Timing diagram showing Access Pause Reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS} −0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified.

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	T_{amb} = −25 to +70 °C
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to +70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = HIGH; notes 2, 3
	I_{DD}	–	50	100	μA	CE = HIGH; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	5	μA	CE = LOW; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V; T_{amb} = −25 to +70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		1,8 V ⩽ V_{DD} ⩽ 6 V
Input leakage current; CE LOW	$-I_{IL}$	–	–	50	nA	CE = LOW
HIGH	I_{IH}	–	–	50	nA	CE = HIGH
Pull-up input current M/S	$-I_{IL}$	30	100	300	nA	V_I = V_{SS}
Pull-down input current F01, F02	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	V_I = V_{SS}

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 8 and 9 < 3 pF.
4. Guarantees correct keyboard operation.

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.		conditions
Outputs M1, DP						
sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V
Latch output HOLD/APO						
sink current	I_{OL}	50	130	300	μA	V_{OL} = 0,5 V
source current	$-I_{OH}$	45	110	250	μA	V_{OH} = 2,5 V

TIMING DATA

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

input levels of F01 and F02 (V_{SS} = LOW; V_{DD} = HIGH)		V_{F01}	LOW	HIGH	LOW	HIGH		
		V_{F02}	LOW	HIGH	HIGH	LOW (test mode)		conditions (note 4)
		symbol						
Dialling pulse frequency	$1/T_{DP}$	f_{DP}	10,13	15,54	19,42	939,2	Hz	note 1
Dialling pulse period	$1/f_{DP}$	T_{DP}	98,7	64,4	51,5	1,073	ms	
Clock pulse frequency	$30 \times f_{DP}$	f_{CL}	303,9	466,1	582,6	27965	Hz	
Break time (note 2)	$3/5 \times T_{DP}$	t_b	59,2	38,6	30,9	0,644	ms	M/S = H; n.c.
Make time (note 2)	$2/5 \times T_{DP}$	t_m	39,5	25,8	20,6	0,429	ms	M/S = H; n.c.
Break time (note 3)	$2/3 \times T_{DP}$	t_b	65,8	42,9	34,6	0,715	ms	M/S = L
Make time (note 3)	$1/3 \times T_{DP}$	t_m	32,9	21,5	17,2	0,358	ms	M/S = L
Inter-digit pause	$8 \times T_{DP}$	t_{id}	790	515	412	8,58	ms	
Reset delay time	$1,6 \times T_{DP}$	t_{rd}	158	103	82,4	1,72	ms	
Access pause time	$32 \times T_{DP}$	t_{ap}	3,16	2,06	1,65	0,034	s	
Prepulse duration	$1/3 \times T_{DP}$	t_d	33	21,5	17,2	0,358	ms	
Debounce time								
min	$4/30 \times T_{DP}$	$t_{e\,min}$	13,2	8,58	6,87	0,143	ms	
max.	$1/6 \times T_{DP}$	$t_{e\,max}$	16,5	10,7	8,58	0,179	ms	
Clock start-up time		$t_{on\,typ}$	4	–	–	–	ms	CE: $V_{SS} \rightarrow V_{DD}$ (note 5)
Initial data entry time (typ.)	$t_{on} + t_e$	t_i	18	14	12	4	ms	

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. Mark-to-space ratio: 3:2.
3. Mark-to-space ratio: 2:1.
4. In the n.c. (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/pull-down current.
5. Stray capacitance between pins 8 and 9: < 3 pF.

TYPICAL CURVES

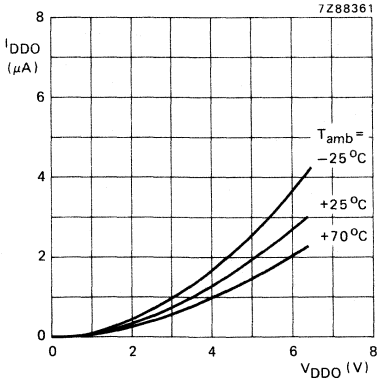


Fig. 11 Standby supply current as a function of standby supply voltage.

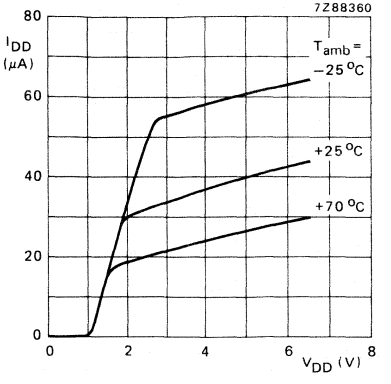


Fig. 12 Operating supply current as a function of operating supply voltage.

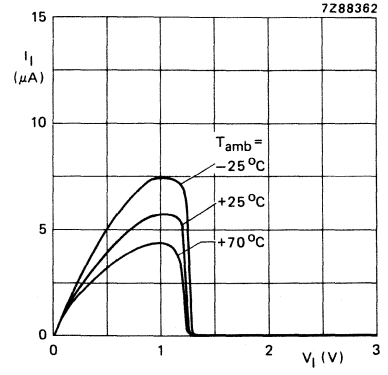


Fig. 13 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

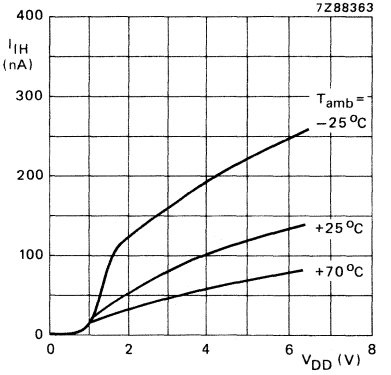


Fig. 14 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

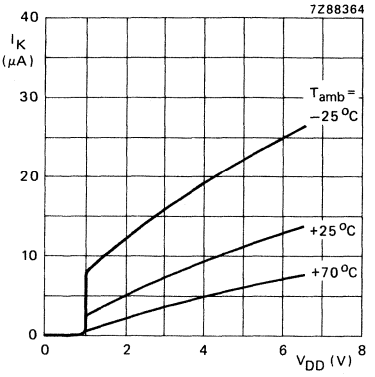


Fig. 15 Keyboard current as a function of supply voltage; X-pins connected to Y-pins.

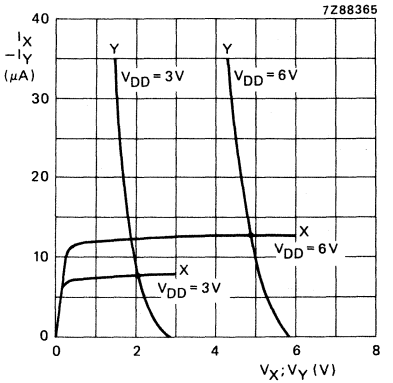


Fig. 16 Keyboard input characteristics at T_{amb} = 25 °C.

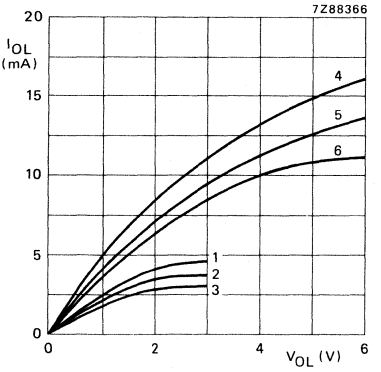


Fig. 17 Output (N-channel) sink characteristics for M1 and DP.

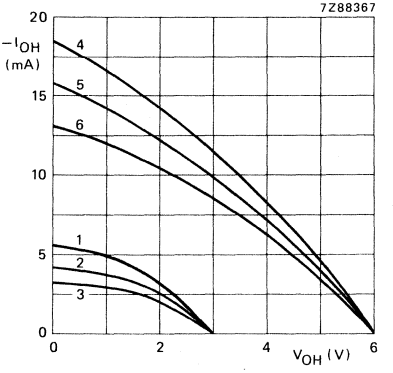


Fig. 18 Output (P-channel) source characteristics for M1 and DP.

Curves for Figs 17 and 18

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3322 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- All inputs with pull-up/pull-down (except CE).
- 23-digit capacity for redial operation.
- Circuit reset for line power breaks; $>$ 160 ms.
- Dialling pulse frequency: 10 Hz.
- Test pulse frequency: 932 Hz.
- Hold facility for lengthening the inter-digit period.
- Memory overflow possibility (with internally disabled redial.
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINES

PCD3322P: 18-lead DIL; plastic (SOT-102G).
PCD3322D: 18-lead DIL; ceramic (SOT-133).

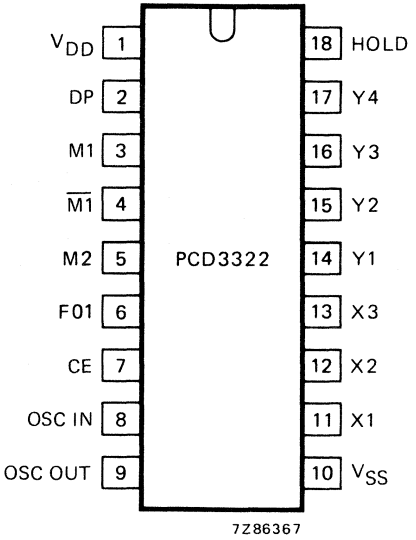


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

6	F01	the dialling pulse frequency is defined by the logic state of this input
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks.
11	X1	column keyboard inputs with pull-down on chip
12	X2	
13	X3	
14	Y1	row keyboard inputs with pull-up on chip
15	Y2	
16	Y3	
17	Y4	
18	HOLD	interrupts dialling after completion of the current digit or immediately following an inter-digit pause (t_{id}); further keyboard data will be accepted

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	M1	Muting; normally used for muting during the dialling sequence
4	$\overline{M1}$	inverted output of M1
5	M2	strobe; HIGH during pulsing of each digit, LOW during an inter-digit pause

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

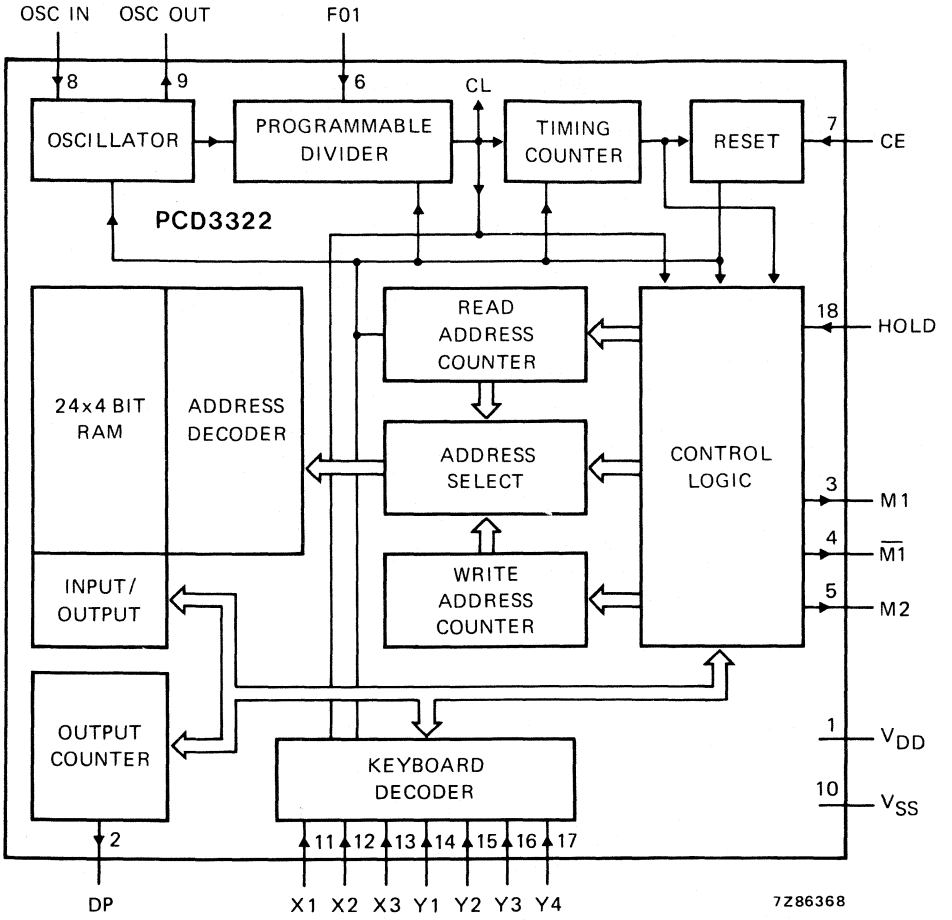


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the PCD3322 is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set by input F01 to provide one of two chip system clocks; the 'normal' clock frequency (F01 = LOW) and the test frequency (F01 = HIGH).

Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

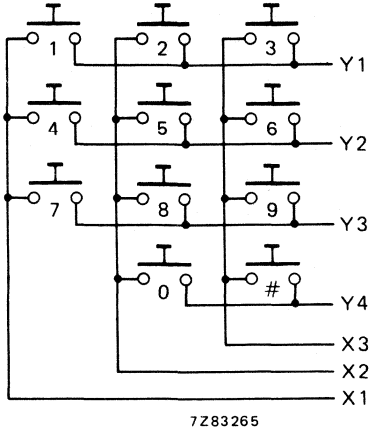
Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig.3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored in the RAM and converted into correctly timed dialling pulses.



Redial.

Fig. 3 Single contact keyboard.

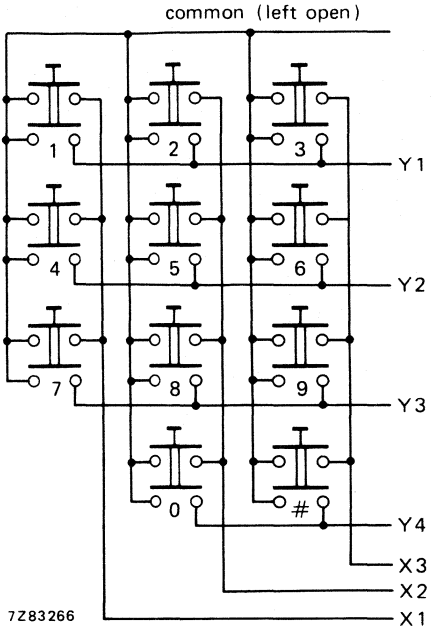


Fig. 4 Double contact keyboard.

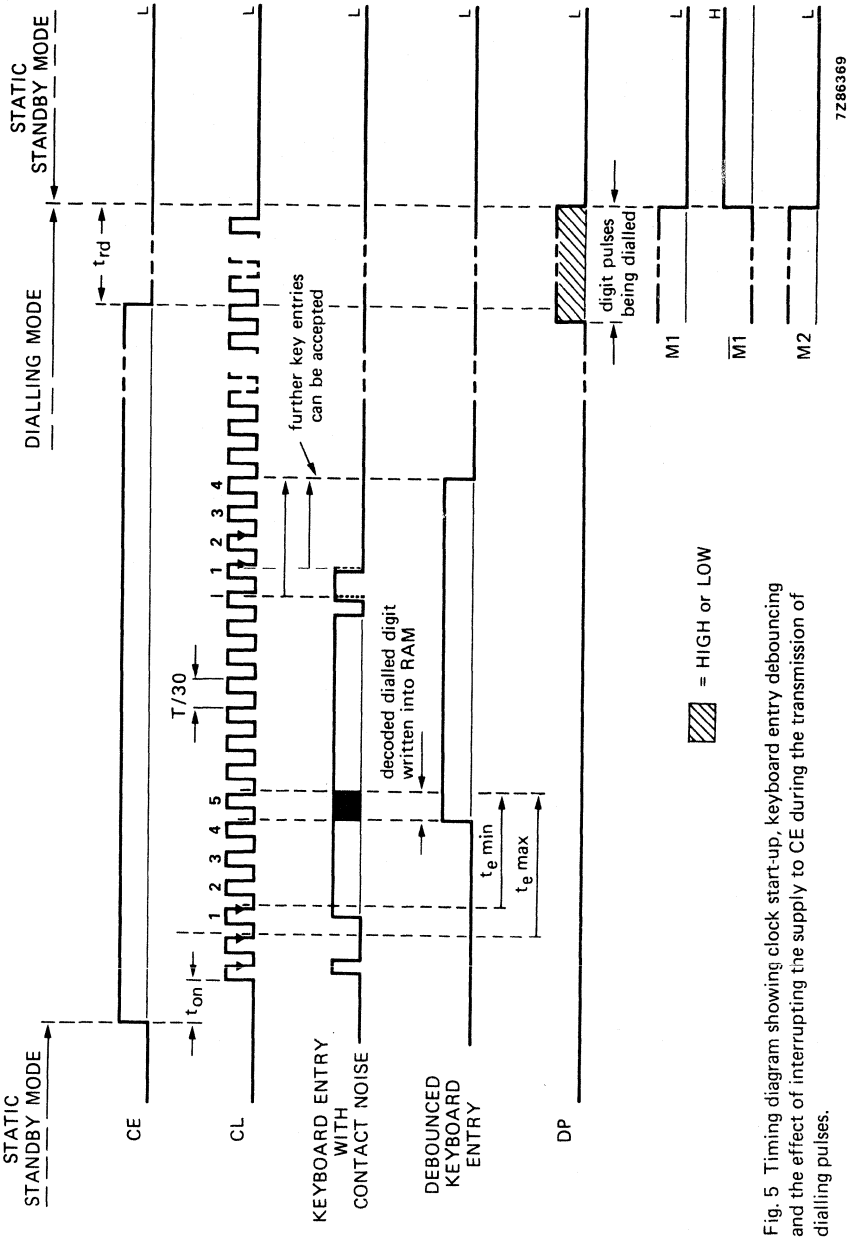


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

N.B.: CL is an internal signal.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at output M1. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse-generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH, the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

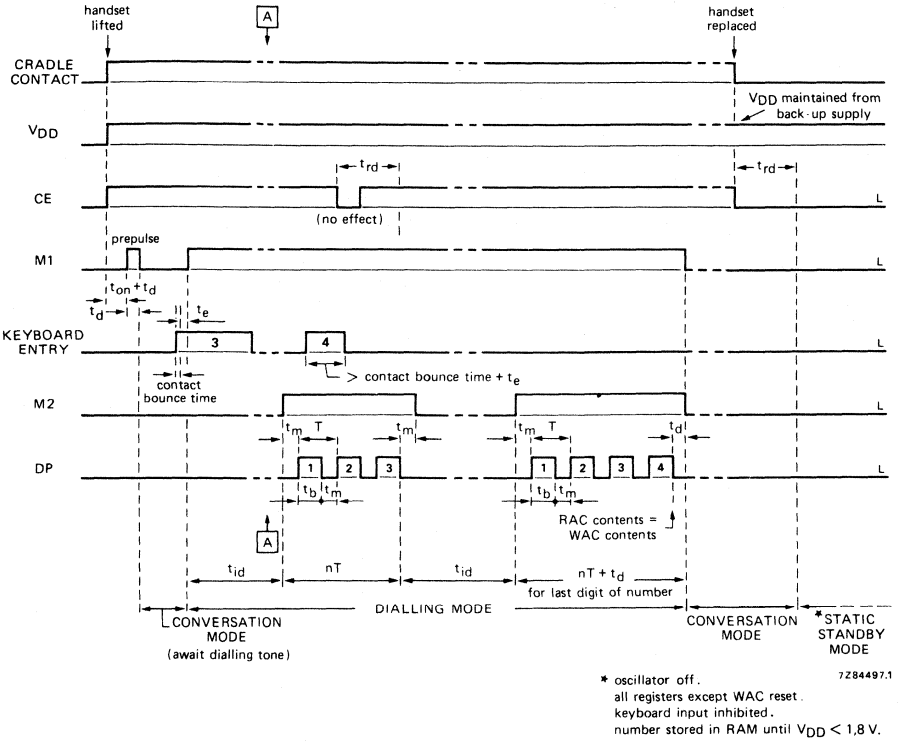


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts).

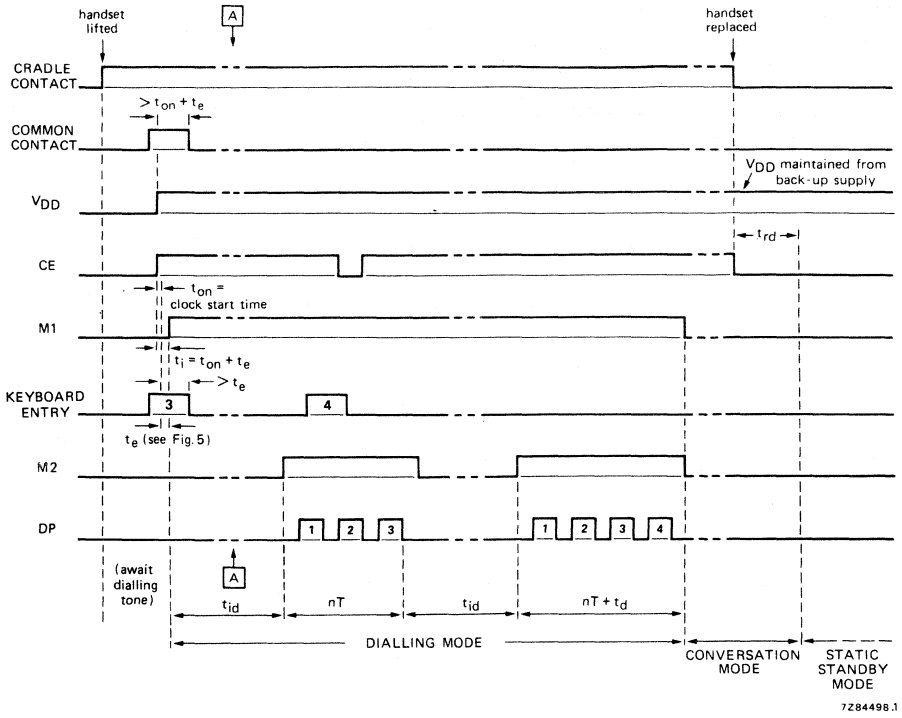


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD input is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on DP until the HOLD input is set LOW again and an inter-digit pause has elapsed.

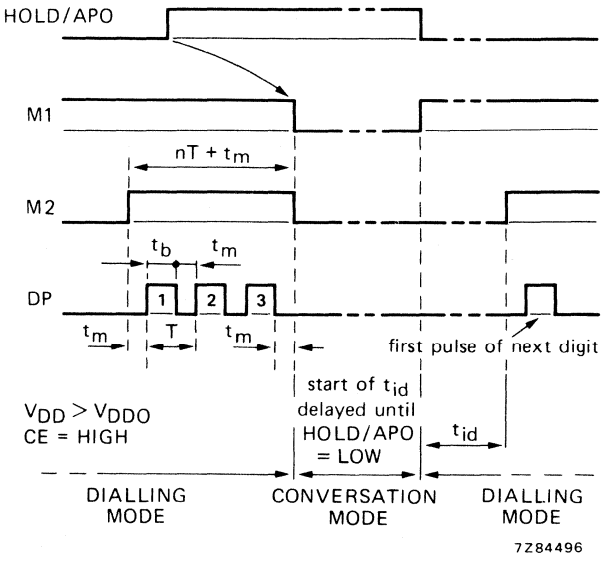


Fig. 8 Timing diagram showing the effect of activating the HOLD input during the transmission of dialling pulses.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS}−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	T_{amb} = −25 to + 70 °C
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to + 70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = HIGH; notes 2, 3
	I_{DD}	–	50	100	μA	CE = HIGH; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	5	μA	CE = LOW; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V; T_{amb} = −25 to + 70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		1,8 V ⩽ V_{DD} ⩽ 6 V
Input leakage current; CE						
LOW	$-I_{IL}$	–	–	50	nA	CE = LOW
HIGH	I_{IH}	–	–	50	nA	CE = HIGH
Pull-down input current F01, HOLD	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	V_I = V_{SS}
Output sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
Output source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 8 and 9 < 3 pF.
4. Guarantees correct keyboard operation.

TIMING DATA I

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz; R_{Smax} = 100 Ω

	symbol	min.	typ.	max.		conditions
Clock start-up time	t_{on}	–	4	–	ms	Figs 6, 7; note 1
Initial data entry time ($t_i = t_{on} + t_e$)	$t_{i\,min}$	–	18	–	ms	F01 = LOW } Fig. 7
	$t_{i\,max}$	–	4	–	ms	F01 = HIGH } Fig. 7

TIMING DATA II (exact values)

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,58 MHz

	symbol	F01 = LOW (dialling)	F01 = HIGH (testing)		conditions
Dialling pulse frequency	f_{DP}	10,13	932,2	Hz	note 2
Dialling pulse period; $1/f_{DP}$	T_{DP}	98,7	1,073	ms	Figs 6, 7
Prepulse duration; 1/3 x T_{DP}	t_d	33	0,358	ms	Figs 6, 7
Inter-digit pause; 8 x T_{DP}	t_{id}	790	8,58	ms	Figs 6, 7
Break time; 3/5 x T_{DP}	t_b	59,2	0,644	ms	Fig. 6
Make time; 2/5 x T_{DP}	t_m	39,5	0,429	ms	Fig. 6
Debounce time					
min. 4/30 x T_{DP}	$t_{e\,min}$	13,2	0,143	ms	Fig. 5
max.; 1/6 x T_{DP}	$t_{e\,max}$	16,5	0,179	ms	Fig. 5
Reset delay time; 1,6 x T_{DP}	t_{rd}	158	1,7	ms	Figs 5, 6, 7

Notes

1. Stray capacitance between pins 8 and 9 < 3 pF.
2. Exactly 10 Hz and 920 Hz respectively when a 3,5328 MHz crystal is used.

TYPICAL CURVES

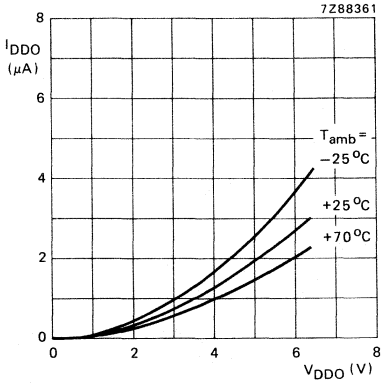


Fig. 9 Standby supply current as a function of standby supply voltage.

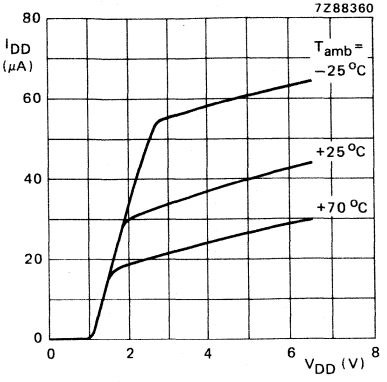


Fig. 10 Operating supply current as a function of operating supply voltage.

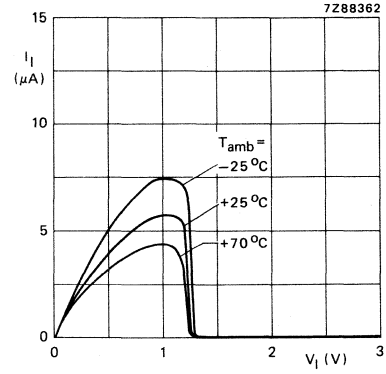


Fig. 11 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

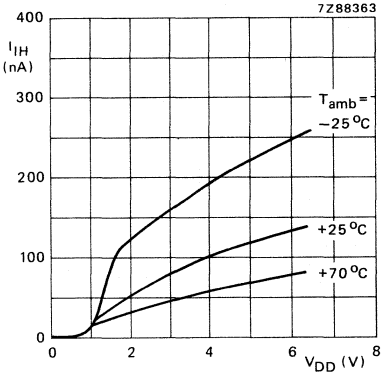


Fig. 12 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

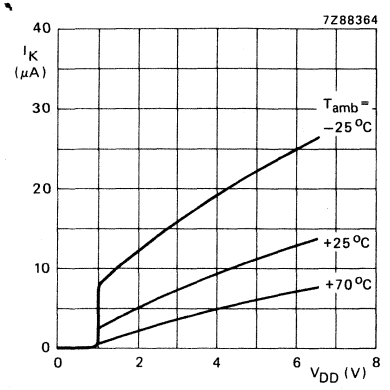


Fig. 13 Keyboard current as a function of supply voltage; X-pins connected to Y-pins.

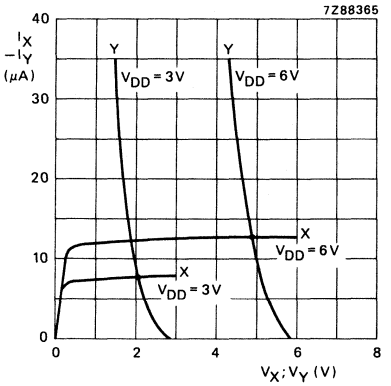


Fig. 14 Keyboard input characteristics at T_{amb} = 25 °C.

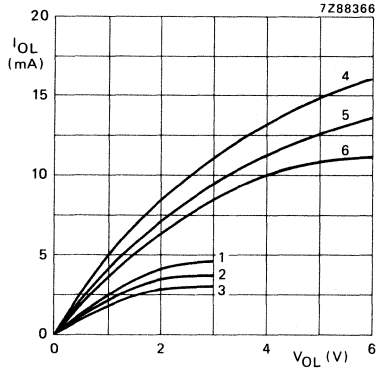


Fig. 15 Output (N-channel) sink characteristics for M1, $\overline{M1}$, M2 and DP.

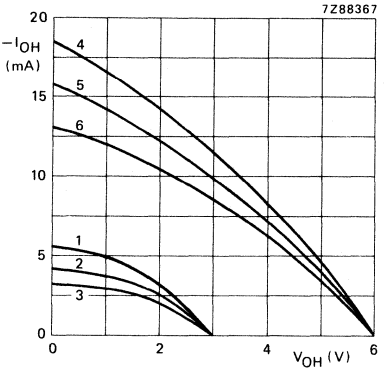


Fig. 16 Output (P-channel) source characteristics for M1, $\overline{M1}$, M2 and DP.

Curves for Figs 15 and 16

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3323 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The PCD3323 can regenerate access pauses during redial. During the original entry, access pauses are stored either automatically or via the keyboard. A regenerated access pause can be terminated during redial in three ways: automatically after a built-in time, or via the keyboard, or with an external dial tone recogniser circuit. This makes the circuit very suitable for redial in PABX (Private Automatic Branch Exchange) systems.

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- 23-digit capacity, including access pauses, for redial operation.
- Memory overflow possibility (with internally disabled redial).
- Selectable dialling pulse frequency: 10 Hz, 16 Hz and 20 Hz.
- Test pulse frequency: 932 Hz.
- Selectable dialling pulse mark/space ratios; 2 : 1 or 3 : 2.
- Selectable inter-digit pause (t_{id}); 8 or 9 times the pulse period (T_{DP}).
- Hold facility for lengthening the inter-digit period.
- Selectable circuit reset for line power breaks; $>$ 160 ms or $>$ 320 ms (10 Hz dialling pulse frequency).
- Access pause generation automatically or via the keyboard.
- Access pause reset:
  automatically after 3 s or 6 s (10 Hz dialling pulse frequency),
  via the keyboard,
  with external tone recogniser.
- All inputs with pull-up/pull-down (except CE).
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINES

PCD3323P: 28-lead DIL; plastic (SOT-117D).
PCD3323D: 28-lead DIL; ceramic (SOT-135).
PCD3323T: 28-lead flat pack; plastic (SO-28; SOT-136A).

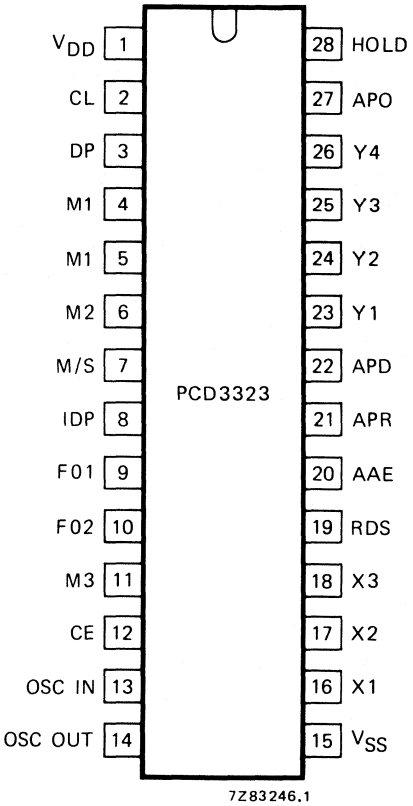


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
15	V_{SS}	negative supply

Inputs

7	M/S	controls the mark-to-space ratio of the line pulses
8	IDP	Inter-Digit-Pause; this occurs before each digit appears at the line output; the duration (t_{id}) can be controlled with this pin
9	F01	the dialling pulse frequency is defined by the logic state of these two inputs
10	F02	
12	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks
16	X1	column keyboard inputs with pull-down on chip
17	X2	
18	X3	
19	RDS	Reset Delay Selection; delay select for chip enable (CE) activity.

20	AAE	Automatic Access Pause Enable; AAE = HIGH: the circuit generates a maximum of two automatic pauses; AAE = LOW: only manual pauses (via keyboard) are possible
21	APR	Access Pause Reset; when any external circuit makes APR = HIGH, a current access pause will be terminated
22	APD	Access Pause Delay; selects the maximum duration of an access pause if no external Access Pause Reset appears.
23	Y1	row keyboard inputs with pull-up on chip
24	Y2	
25	Y3	
26	Y4	
28	HOLD	interrupts dialling after completion of the current digit or immediately during an inter-digit pause (t_{id}); further keyboard data will be accepted

Outputs

2	CL	output of the internal system clock; external forcing is possible for frequencies not selectable with F01/F02
3	DP	Dialling Pulse; drive of the external line switching transistor or relay
4	$\underline{M1}$	Muting; normally used for muting during the dialling sequence
5	$\overline{M1}$	inverted output of M1
6	M2	strobe; HIGH during pulsing of each digit, LOW during an inter-digit pause
11	M3	AND function, with $\overline{DP}$ and M1 as input, for direct drive of a switching transistor for dialling pulses and muting
27	APO	Access Pause Output; this output will go HIGH when an access pause code is read from the memory during pulsing.

Oscillator

13	OSC IN	input and output of the on-chip oscillator
14	OSC OUT	

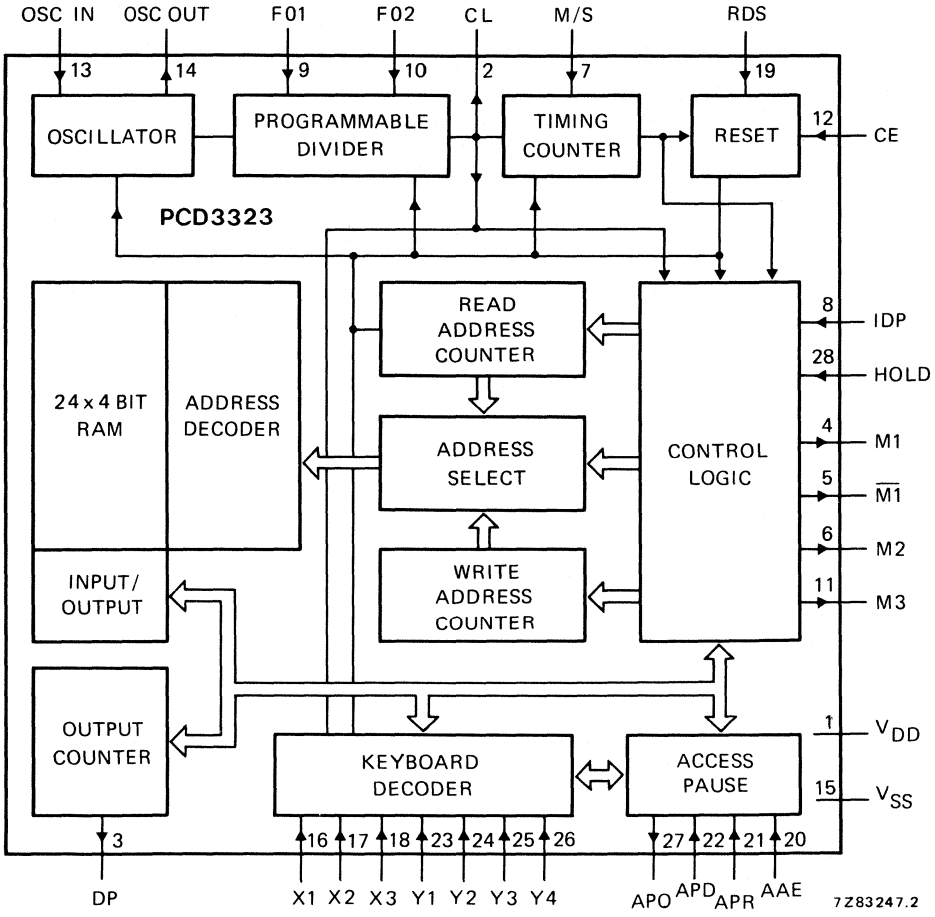


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the PCD3323 is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set (F01 and F02) to provide one of four chip system clocks; three 'normal' clock frequencies and one higher test frequency.
The system clock is available on pin CL and can be used for external logic. External forcing of CL is possible for frequencies which are not selectable with F01/F02.
Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced. The t_{rd} pulse duration is selected by the RDS input.

Debouncing keyboard entries

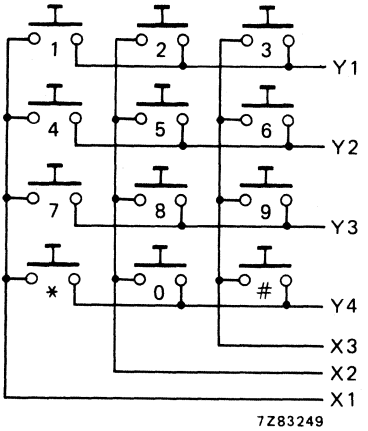
The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC reprents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP.

If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the PCD3323. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.



★ Access pause set.

Redial or Access Pause Reset.

Fig. 3 Single contact keyboard.

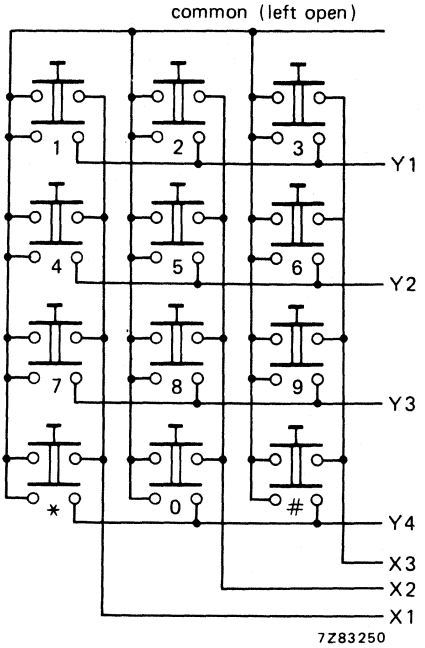


Fig. 4 Double contact keyboard.

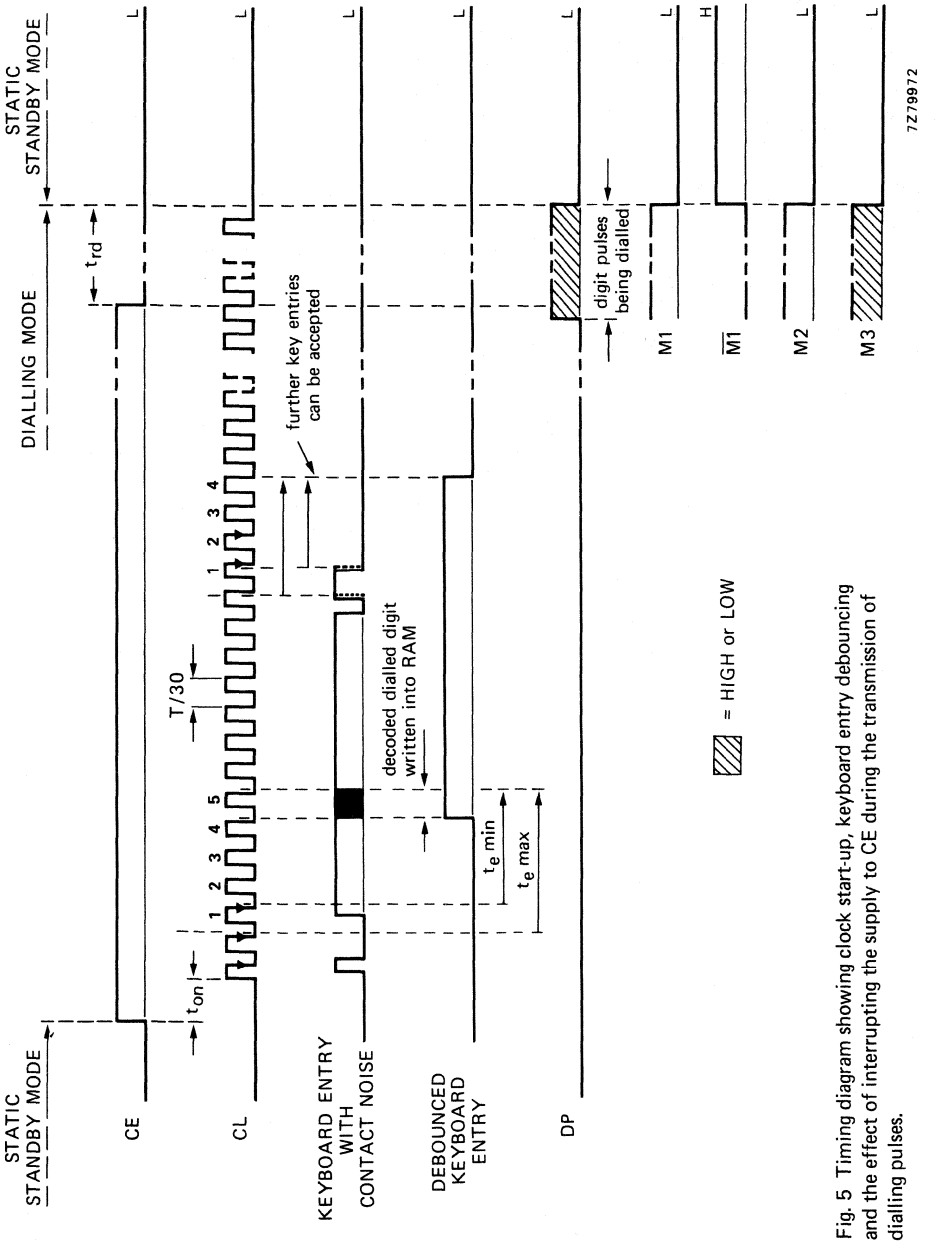


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at outputs M1 and M3. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH, the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at outputs DP and M3. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 or 3,2 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

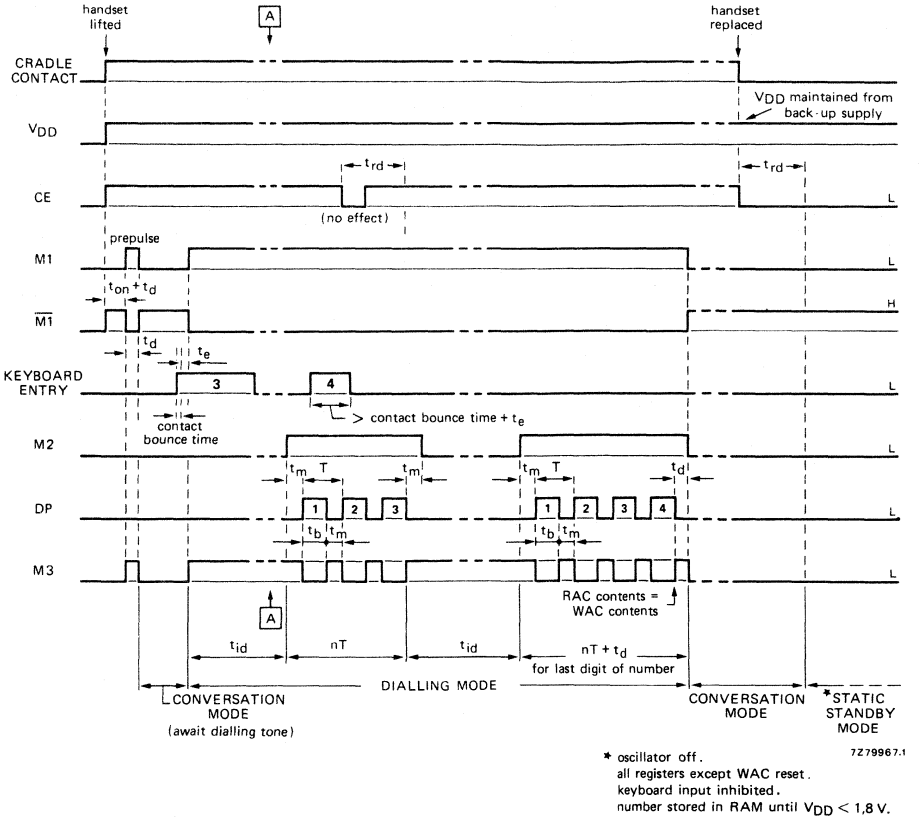


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts).

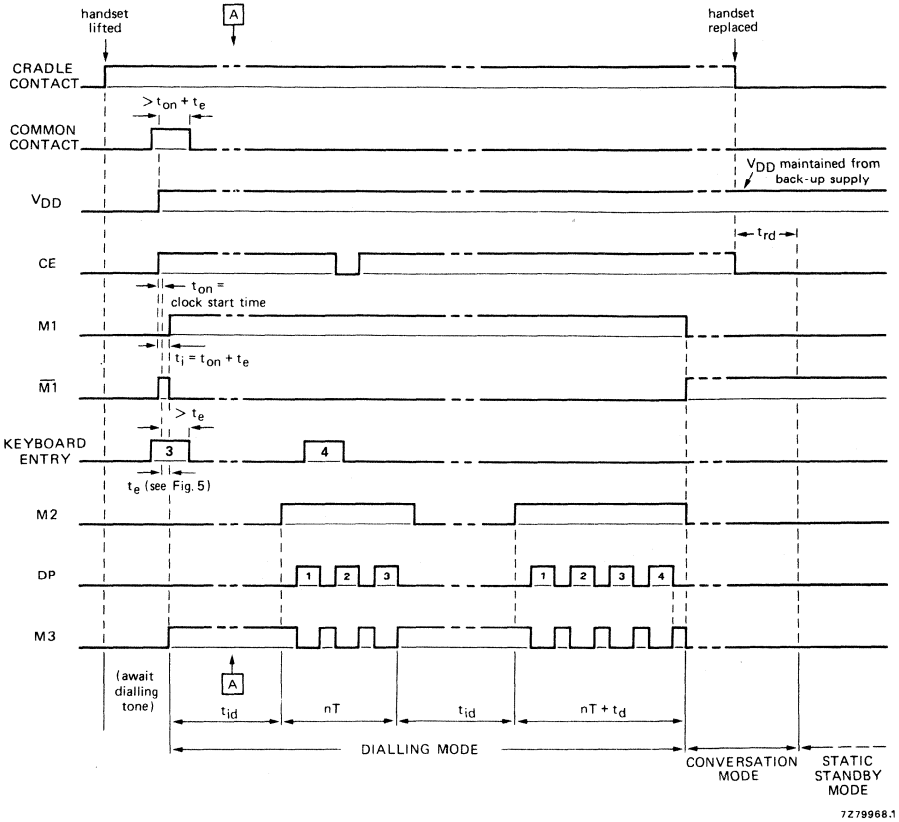


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD input is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on M3 and DP until the HOLD input is set LOW again and an inter-digit pause has elapsed.

HOLD can be controlled by the Access Pause Output (see next section).

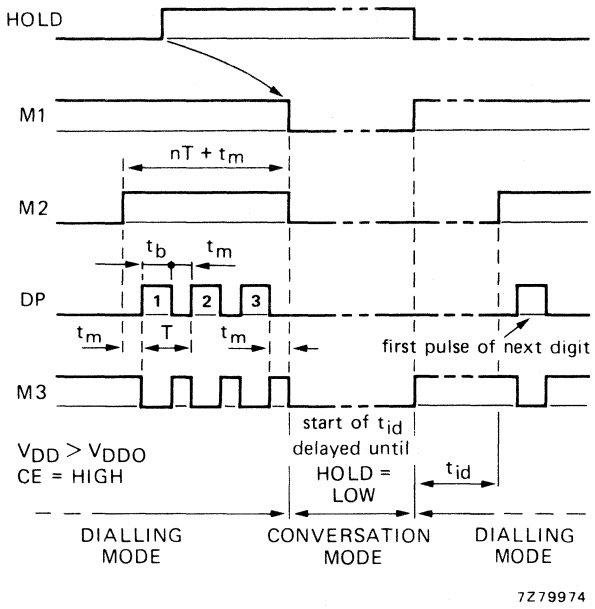


Fig. 8 Timing diagram showing the effect of activating the HOLD input during the transmission of dialling pulses.

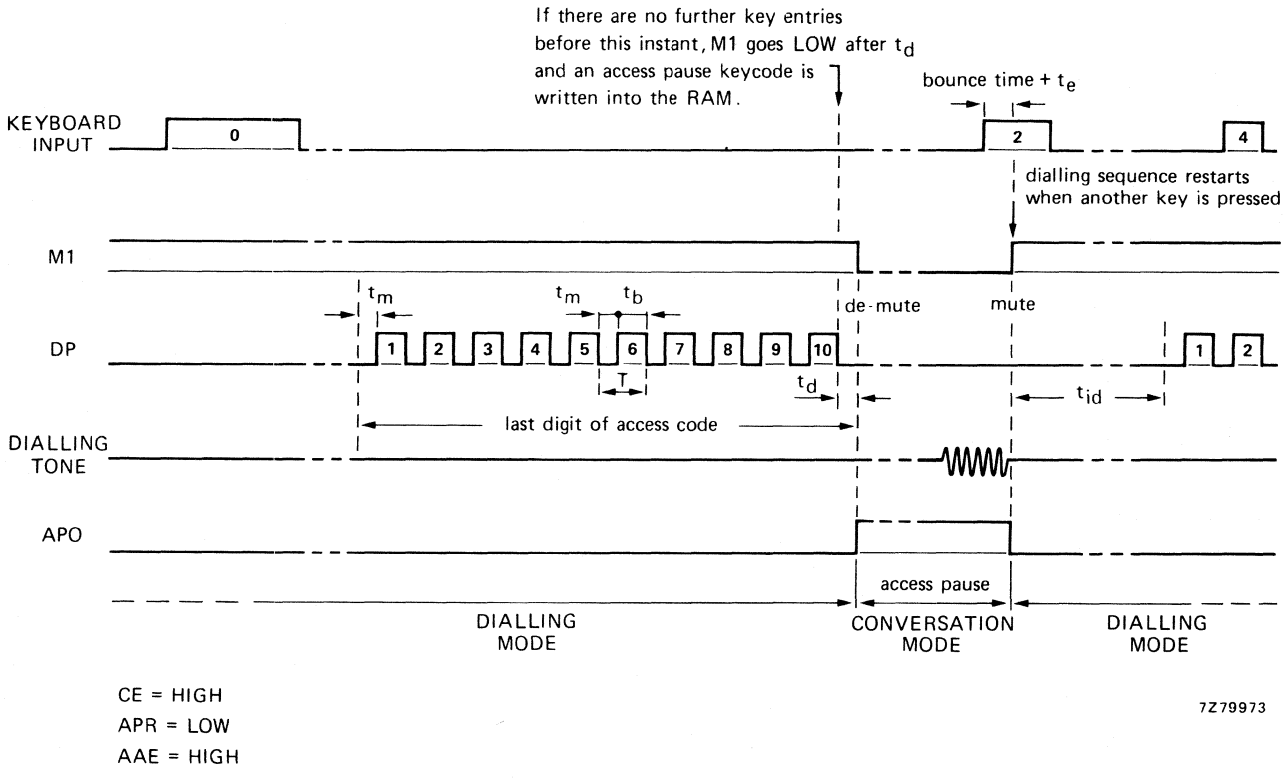


Fig. 9 Dialling sequence showing how an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.

Access pause regeneration during redial

During original entry, access pause codes can be stored at the appropriate positions in the RAM. During redial the Access Pause Output (APO) will go HIGH as soon as an access pause code is read from the RAM. This can be used to make HOLD = HIGH, thereby interrupting dialling until HOLD is made LOW again as described above. In this way the normal inter-digit pause with a duration t_{id} can be replaced by a proper access pause.

Access pause codes can be stored in two ways:

- *Manually,* with AAE and APR both LOW. In this case access pause codes can only be stored by pressing the access pause key (★) between entering the trunk exchange code and the subscriber code, or at any other moment an access pause is required. The number of access pauses that can be inserted in this manner is only limited by the capacity of the RAM (digits + access pauses ⩽ 23).
- *Automatically,* with AAE = HIGH and APR = LOW (see Fig. 9). An access pause code is now automatically stored in the RAM during original entry, when M1 goes LOW, after all digits so far entered have been transmitted (see Fig. 6). This occurs between entering of the trunk exchange code and the subscriber code, whilst the access tone is available. Up to two access pauses can be entered into the RAM in this manner. Alternatively, the access pause key can still be pressed to insert (more) access pauses manually.

During redial, access pauses will be regenerated only if APR = LOW and with APO connected to HOLD; they can be terminated in three ways (see Fig. 10 and next page).

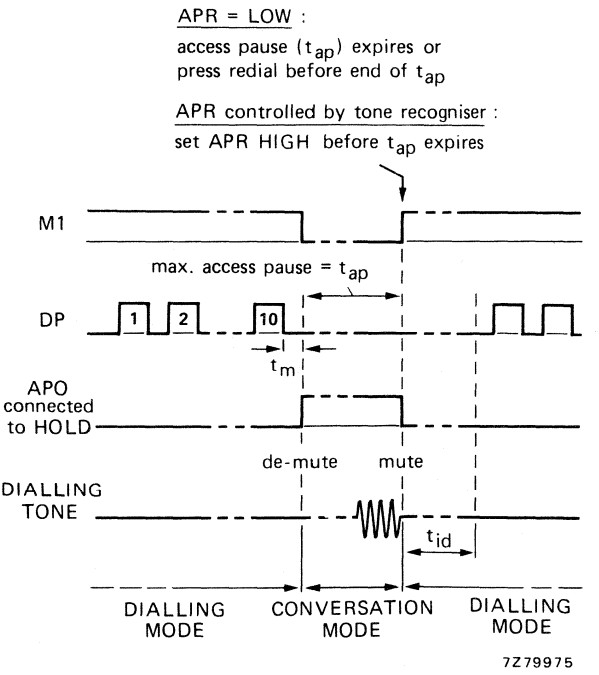


Fig. 10 Timing diagram showing Access Pause Reset for APR = LOW or APR is controlled by tone recogniser.

Three methods of terminating an access pause:

1. Automatically, if the built-in time t_{ap} expires; APO then goes LOW; t_{ap} can be set to one of two values with the Access Pause Delay (APD) select input.
2. Manually, by pressing the redial key before t_{ap} expires.
3. By making APR = HIGH before t_{ap} expires, with an external tone recogniser (see Fig. 11).

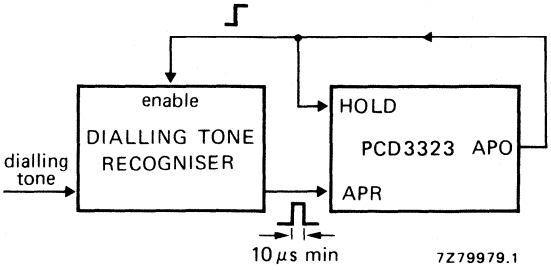


Fig. 11 Circuit for automatic termination of an access pause during redialling by using a tone recogniser to set APR to HIGH for more than 10 μs.

Access pauses longer than t_{ap} can be obtained by connecting APO to HOLD via a latching device. Figure 12 shows a tone recogniser circuit, which automatically terminates access pauses upon receipt of the access tone, whether this is before or after t_{ap} expires.

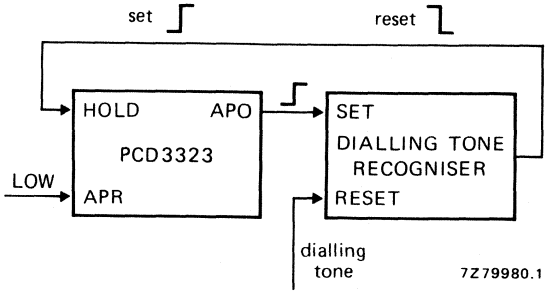


Fig. 12 Circuit for automatically shortening or lengthening an access pause under the control of a tone recogniser. For timing diagram see Fig. 13.

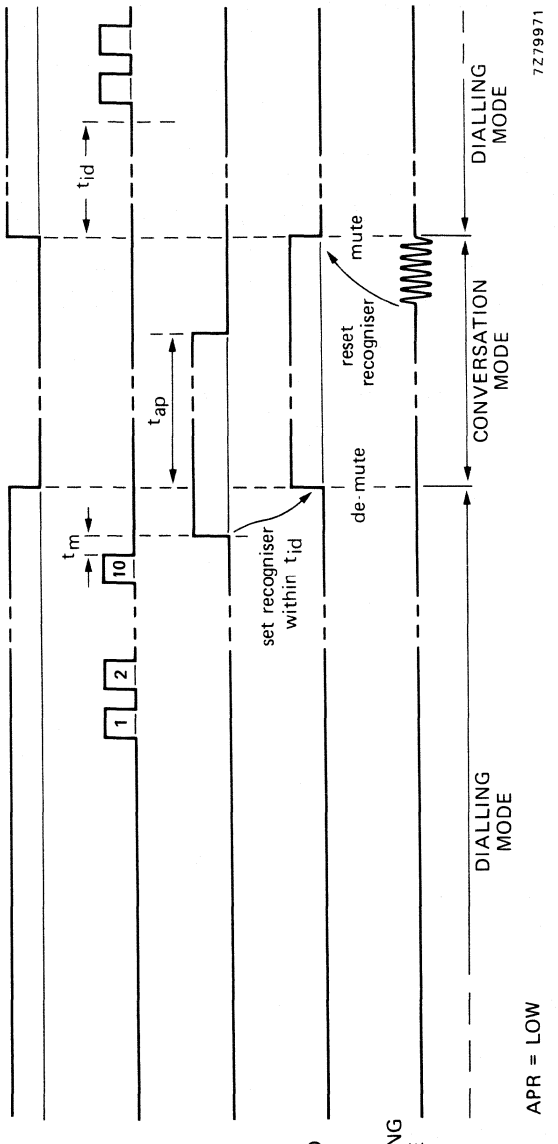


Fig. 13 Timing diagram showing automatic shortening or lengthening an access pause; for the circuit see Fig. 12.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS}−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	T_{amb} = −25 to + 70 °C
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to + 70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = HIGH; notes 2, 3
	I_{DD}	–	50	100	μA	CE = HIGH; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	5	μA	CE = LOW; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V T_{amb} = −25 to + 70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		1,8 V ⩽ V_{DD} ⩽ 6 V
Input leakage current; CE						
LOW	$-I_{IL}$	–	–	50	nA	CE = LOW
HIGH	I_{IH}	–	–	50	nA	CE = HIGH
Pull-up input current M/S, APR	$-I_{IL}$	30	100	300	nA	V_I = V_{SS}
Pull-down input current IDP, F01, F02, HOLD, AAE, ADP, RDS	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	V_I = V_{SS}

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 13 and 14 < 3 pF.
4. Guarantees correct keyboard operation.

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.		conditions
Outputs M1, $\overline{M1}$, M2, M3, DP						
sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V
Outputs CL, APO						
sink current	I_{OL}	50	130	300	μA	V_{OL} = 0,5 V
source current	$-I_{OH}$	45	110	250	μA	V_{OH} = 2,5 V

TIMING DATA

V_{DD} = 3 V; V_{SS} = 0 V; f_{osc} = 3,58 MHz

	symbol	min.	typ.	max.		conditions
Clock start-up time	t_{on}	–	4	–	ms	CE: $V_{SS} \rightarrow V_{DD}$ (note)
APR-hold time	t_{APRH}	10	–	–	μs	see Fig. 11

Note: stray capacitance between pins 13 and 14 < 3 pF.

TIMING DATA (continued)

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

input levels of F01 and F02 (V_{SS} = LOW; V_{DD} = HIGH)		V_{F01}	LOW	HIGH	LOW	HIGH		
		V_{F02}	LOW	HIGH	HIGH	LOW		conditions (note 4)
		symbol				(test mode)		
Dialling pulse frequency	$1/T_{DP}$	f_{DP}	10,13	15,54	19,42	932,2	Hz	note 1
Dialling pulse period	$1/f_{DP}$	T_{DP}	98,7	64,4	51,5	1,073	ms	
Clock pulse frequency	$30 \times f_{DP}$	f_{CL}	303,9	466,1	582,6	27965	Hz	
Break time (note 2)	$3/5 \times T_{DP}$	t_b	59,2	38,6	30,9	0,644	ms	M/S = H; n.c.
Make time (note 2)	$2/5 \times T_{DP}$	t_m	39,5	25,8	20,6	0,429	ms	M/S = H; n.c.
Break time (note 3)	$2/3 \times T_{DP}$	t_b	65,8	42,9	34,6	0,715	ms	M/S = L
Make time (note 3)	$1/3 \times T_{DP}$	t_m	32,9	21,5	17,2	0,358	ms	M/S = L
Inter-digit pause	$8 \times T_{DP}$	t_{id}	790	515	412	8,58	ms	IDP = L; n.c.
	$9 \times T_{DP}$	t_{id}	888	579	463	9,65	ms	IDP = H
Reset delay time	$1,6 \times T_{DP}$	t_{rd}	158	103	82,4	1,72	ms	RDS = L; n.c.
	$3,2 \times T_{DP}$	t_{rd}	316	206	165	3,43	ms	RDS = H
Access pause time	$32 \times T_{DP}$	t_{ap}	3,16	2,06	1,65	0,034	s	APD = L; n.c.
	$64 \times T_{DP}$	t_{ap}	6,32	4,12	3,30	0,069	s	APD = H
Prepulse duration	$1/3 \times T_{DP}$	t_d	33	21,5	17,2	0,358	ms	
Debounce time								
min.	$4/30 \times T_{DP}$	$t_{e\,min}$	13,2	8,58	6,87	0,143	ms	
max.	$1/6 \times T_{DP}$	$t_{e\,max}$	16,5	10,7	8,58	0,179	ms	
Initial data entry time (typ.)	$t_{on} + t_e$	t_i	18	14	12	4	ms	

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. Mark-to-space ratio: 3: 2.
3. Mark-to-space ratio: 2: 1.
4. In the n.c. (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/pull-down current.

TYPICAL CURVES

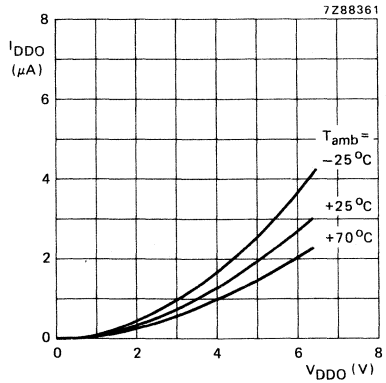


Fig. 14 Standby supply current as a function of standby supply voltage.

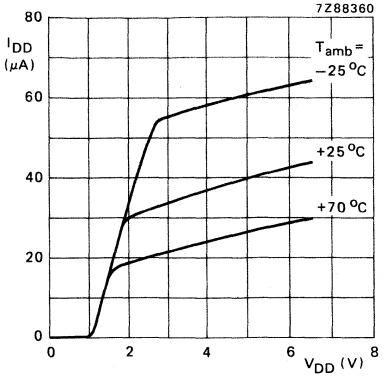


Fig. 15 Operating supply current as a function of operating supply voltage.

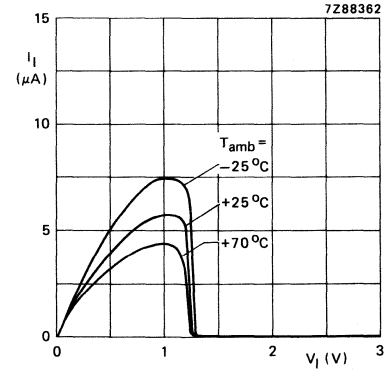


Fig. 16 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

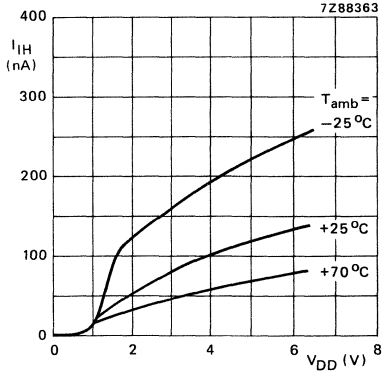


Fig. 17 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

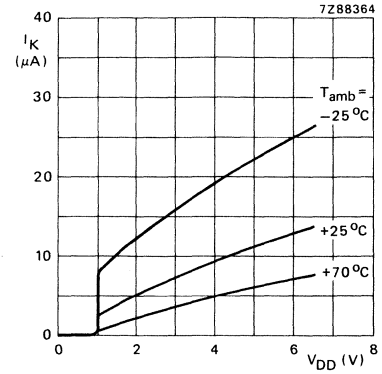


Fig. 18 Keyboard current as a function of supply voltage; X-pins connected to Y-pins.

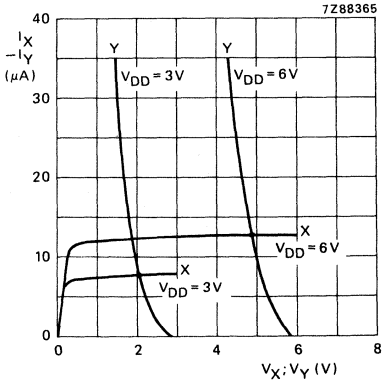


Fig. 19 Keyboard input characteristics at T_{amb} = 25 °C.

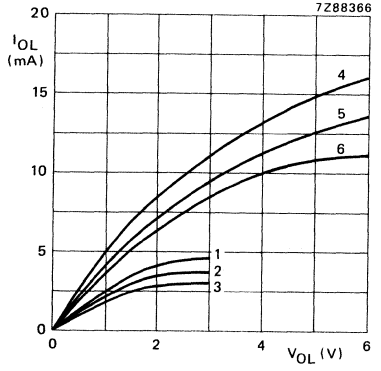


Fig. 20 Output (N-channel) sink characteristics for M1, $\overline{M1}$, M2, M3 and DP.

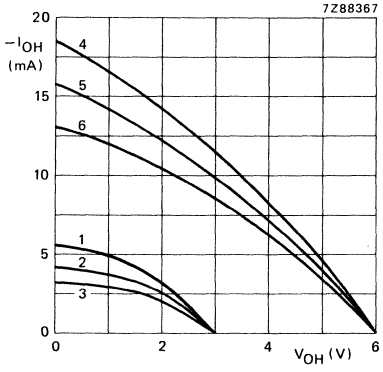


Fig. 21 Output (P-channel) source characteristics for M1, $\overline{M1}$, M2, M3 and DP.

Curves for Figs 20 and 21

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3324 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The PCD3324 can regenerate access pauses during redial. During the original entry, only one access pause is stored automatically or several via the keyboard. A regenerated access pause can be terminated during redial in three ways: automatically after a built-in time, or via the keyboard, or with an external dial tone recogniser circuit. This makes the circuit very suitable for redial in PABX (Private Automatic Branch Exchange) systems. The PCD3324 is pin to pin compatible with the DF320 and the MT4320 (however, including additional functions).

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- 23-digit capacity, including access pauses, for redial operation.
- Memory overflow possibility (with internally disabled redial).
- Selectable dialling pulse frequency: 10 Hz, 16 Hz and 20 Hz.
- Test pulse frequency: 932 Hz.
- Selectable dialling pulse mark/space ratios; 2 : 1 or 3 : 2.
- Hold facility for lengthening the inter-digit period.
- Circuit reset for line power breaks; > 160 ms (10 Hz dialling pulse frequency).
- Access pause generation automatically or via the keyboard.
- Access pause reset:
  automatically after 3 s (10 Hz dialling pulse frequency),
  via the keyboard,
  with external tone recogniser.
- All inputs with pull-up/pull-down (except CE).
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINES

PCD3324P : 18-lead DIL; plastic (SOT-102G).
PCD3324D: 18-lead DIL; ceramic (SOT-133).

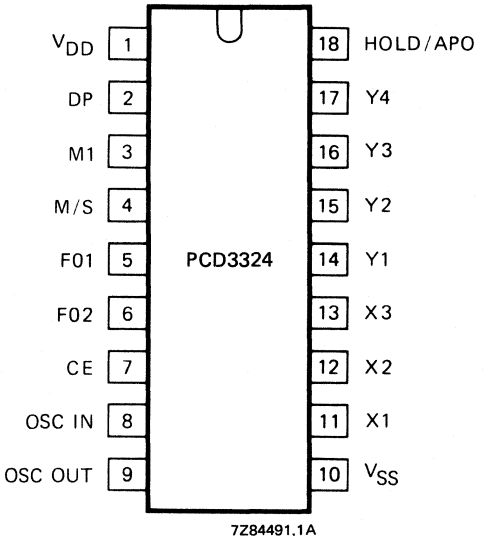


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

4	M/S	controls the mark-to-space ratio of the line pulses
5	F01	the dialling pulse frequency is defined by the logic state of these two inputs
6	F02	
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks
11	X1	column keyboard inputs with pull-down on chip
12	X2	
13	X3	
14	Y1	row keyboard inputs with pull-up on chip
15	Y2	
16	Y3	
17	Y4	

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	M1	Muting; normally used for muting during the dialling sequence

Input/output

18	HOLD/APO	This pin will go HIGH when an access pause code is read from the memory during pulsing and will interrupt dialling. It can also be externally controlled; it will interrupt dialling after completion of the current digit or immediately during an inter-digit pause (t_{id}); further keyboard data will be accepted.

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

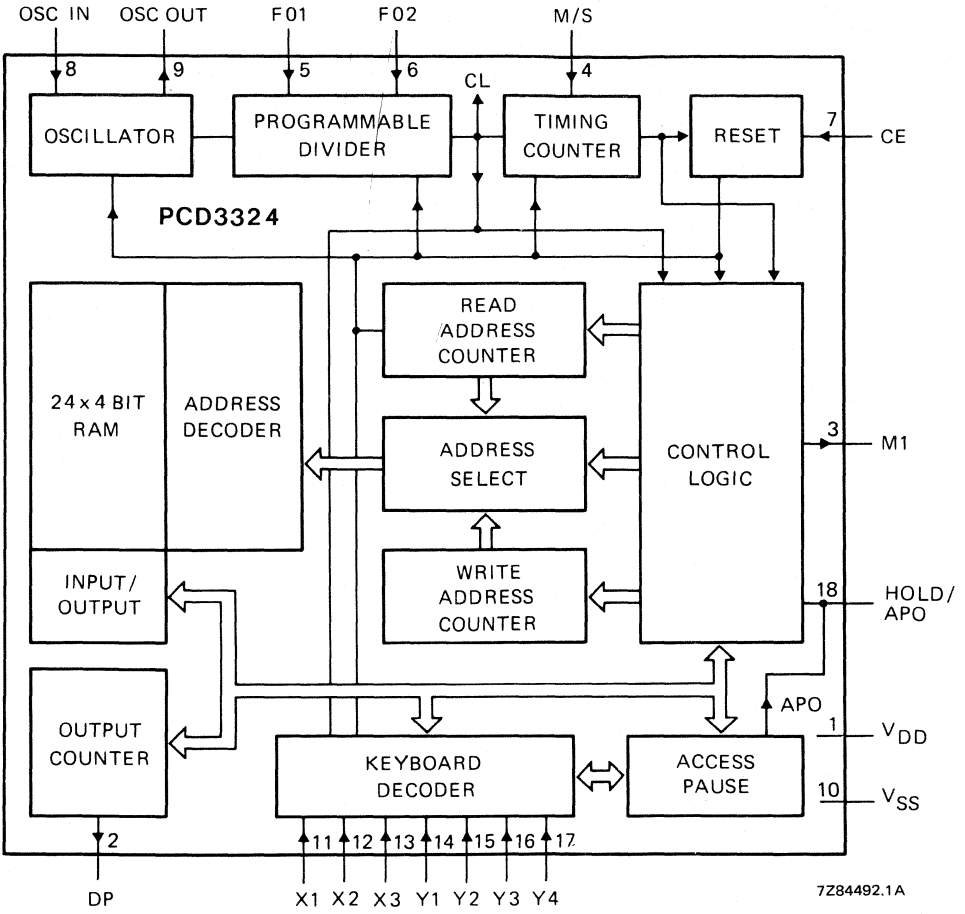


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the **PCD3324** is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set (F01 and F02) to provide one of four chip system clocks; three 'normal' clock frequencies and one higher test frequency.

Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

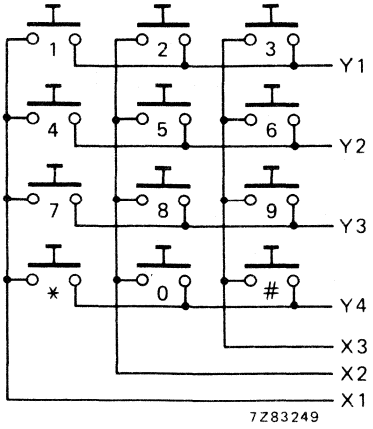
Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the PCD3324. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.



★ Access pause set.

Redial or Access Pause Reset.

Fig. 3 Single contact keyboard.

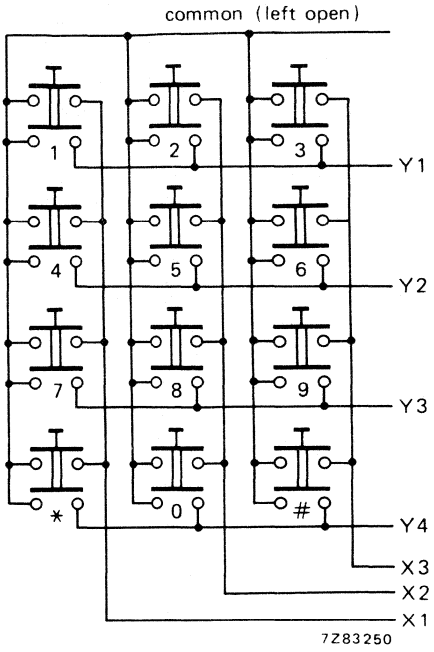


Fig. 4 Double contact keyboard.

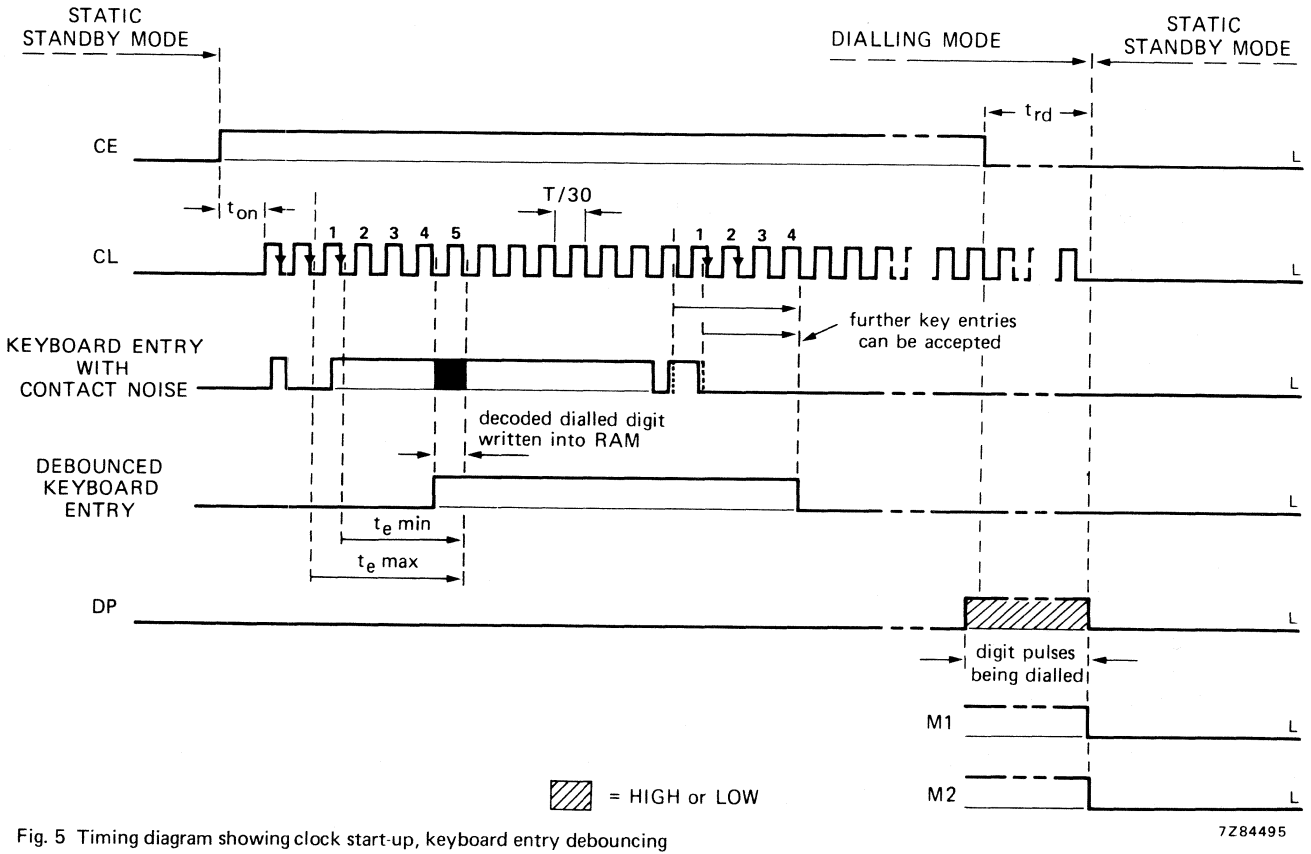


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

N.B.: CL and M2 are internal signals.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at output M1. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

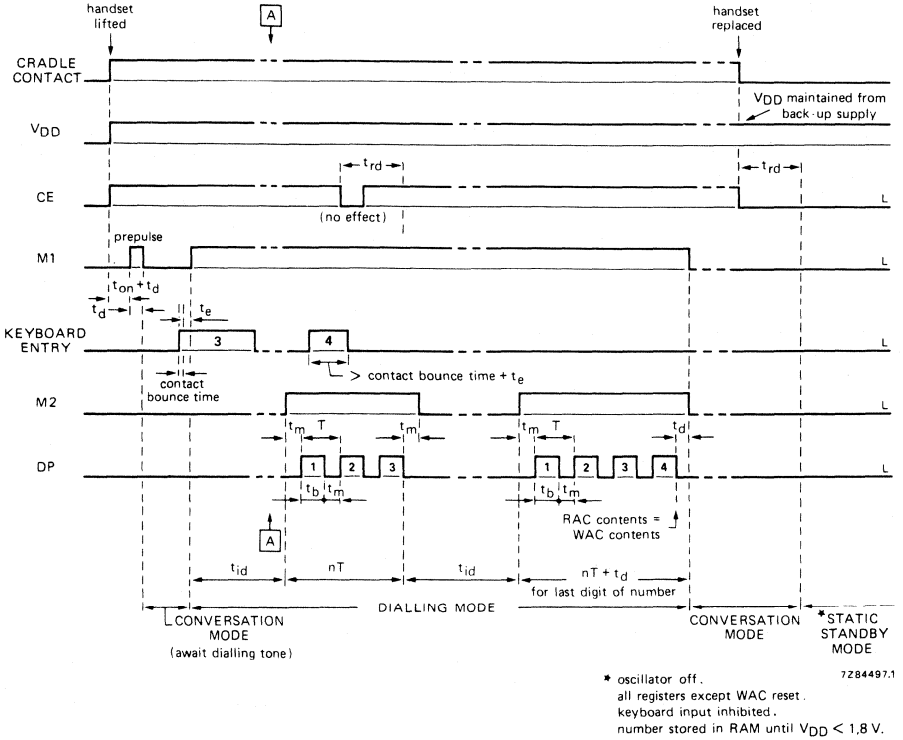


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.

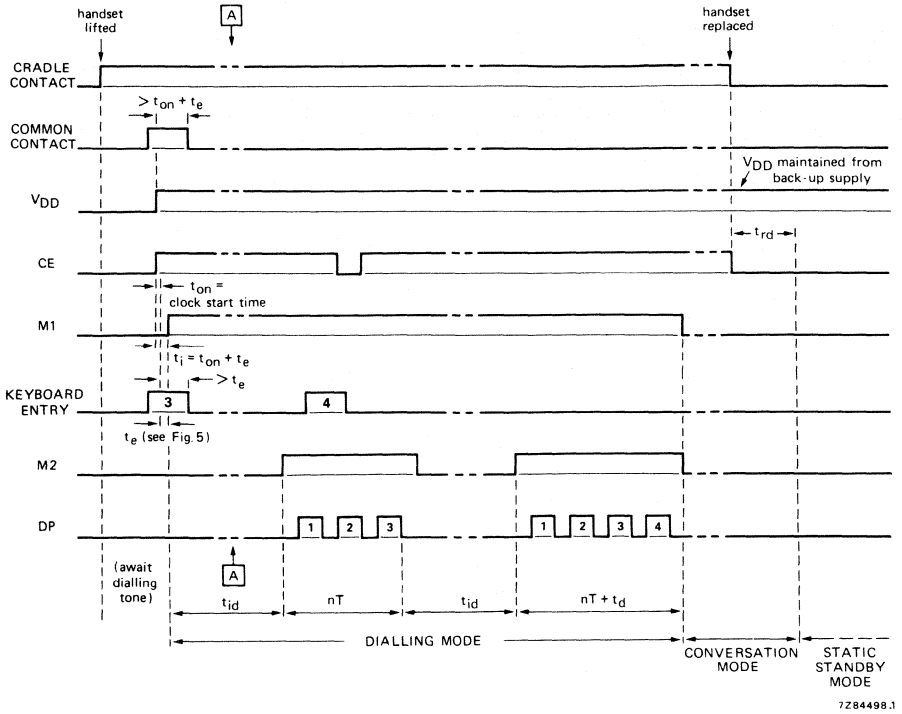


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A. M2 is an internal signal.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD/APO is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on DP until the HOLD/APO is set LOW again and an inter-digit pause has elapsed.

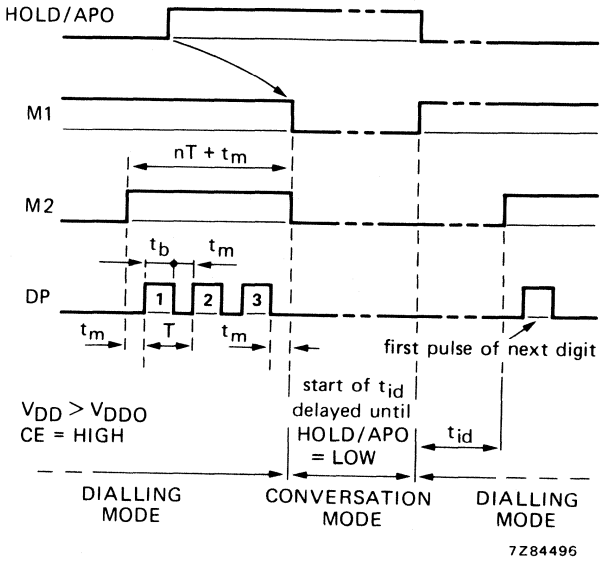


Fig. 8 Timing diagram showing the effect of activating the HOLD/APO during the transmission of dialling pulses. M2 is an internal signal.

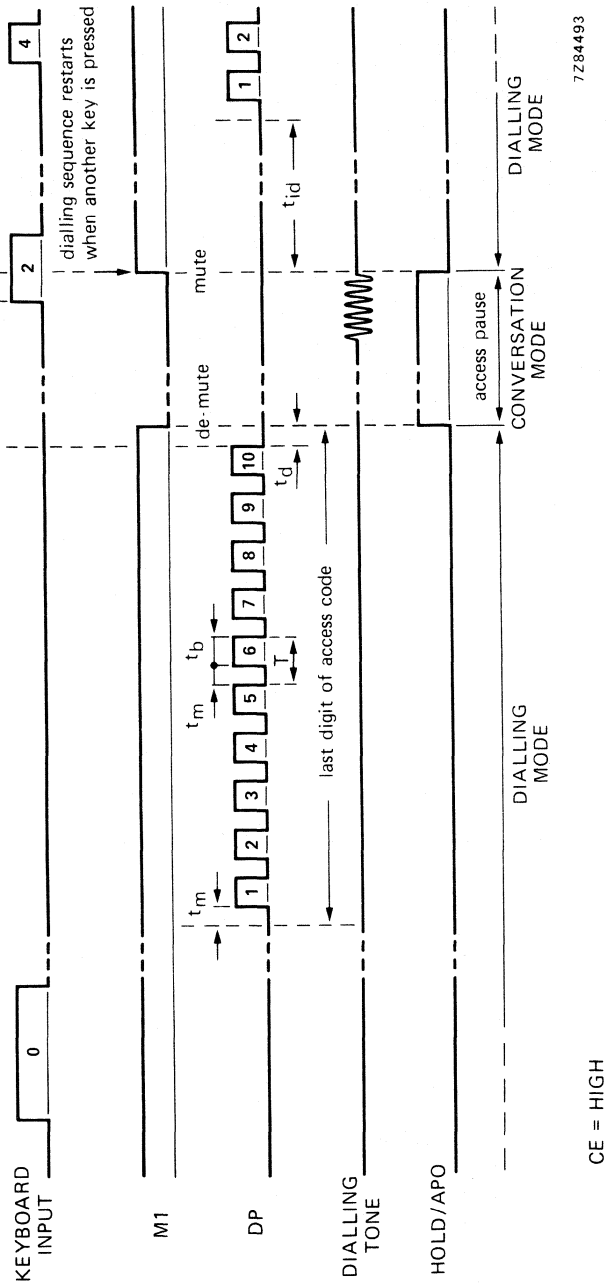
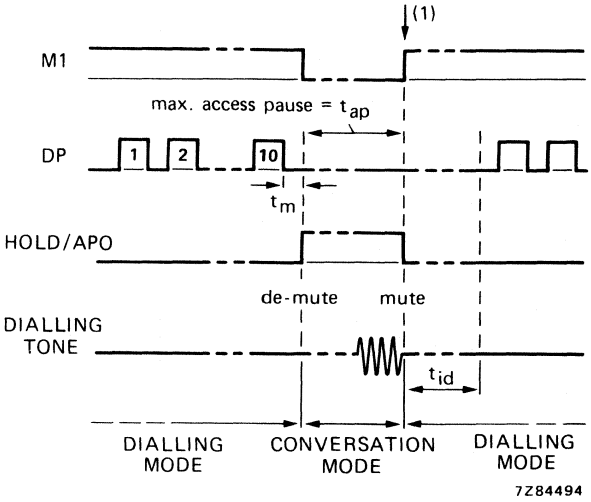


Fig. 9 Dialling sequence showing how an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.

Access pause regeneration during redial

During original entry, access pause codes can be stored at the appropriate positions in the RAM. During redial the Access Pause Output (HOLD/APO)will go HIGH as soon as an access pause code is read from the RAM, thereby interrupting dialling until HOLD/APO is made LOW again as described above. In this way the normal inter-digit pause with a duration t_{id} can be replaced by a proper access pause. An access pause code is now automatically stored in the RAM during original entry, when M1 goes LOW, after all digits so far entered have been transmitted (see Fig. 6). This occurs between entering of the trunk exchange code and the subscriber code, whilst the access tone is available. Only one access pause can be entered into the RAM in this manner. Alternatively, the access pause key (★) can still be pressed to insert (more) access pauses manually (digits.+ access pauses ⩽ 23).
During redial, access pauses will be automatically regenerated.

Three methods of terminating an access pause:
1. Automatically, if the built-in time t_{ap} expires; HOLD/APO then goes LOW.
2. Manually, by pressing the redial key before t_{ap} expires.
3. With an external tone recogniser, by forcing HOLD/APO to LOW or HIGH respectively, for shortening or lengthening an access pause.



(1) a. Access pause (t_{ap}) expires or press redial before end of t_{ap}.

b. HOLD/APO controlled by tone recogniser:
HOLD/APO forced to LOW before t_{ap} expires; access pause $< t_{ap}$
HOLD/APO forced to HIGH after t_{ap} expires; access pause $> t_{ap}$.

Fig. 10 Timing diagram showing Access Pause Reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS}−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified.

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	T_{amb} = −25 to +70 °C
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to +70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = HIGH; notes 2, 3
	I_{DD}	–	50	100	μA	CE = HIGH; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	2	μA	CE = LOW; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V; T_{amb} = −25 to +70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		1,8 V ⩽ V_{DD} ⩽ 6 V
Input leakage current; CE LOW	$-I_{IL}$	–	–	50	nA	CE = LOW
HIGH	I_{IH}	–	–	50	nA	CE = HIGH
Pull-up input current M/S	$-I_{IL}$	30	100	300	nA	V_I = V_{SS}
Pull-down input current F01, F02	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	V_I = V_{SS}

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 8 and 9 < 3 pF.
4. Guarantees correct keyboard operation.

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.		conditions
Outputs M1, DP						
sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V
Latch output HOLD/APO						
sink current	I_{OL}	50	130	300	μA	V_{OL} = 0,5 V
source current	$-I_{OH}$	45	110	250	μA	V_{OH} = 2,5 V

TIMING DATA

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

input levels of F01 and F02 (V_{SS} = LOW; V_{DD} = HIGH)		V_{F01}	LOW	HIGH	LOW	HIGH		
		V_{F02}	LOW	HIGH	HIGH	LOW		conditions (note 4)
		symbol				(test mode)		
Dialling pulse frequency	$1/T_{DP}$	f_{DP}	10,13	15,54	19,42	939,2	Hz	note 1
Dialling pulse period	$1/f_{DP}$	T_{DP}	98,7	64,4	51,5	1,073	ms	
Clock pulse frequency	$30 \times f_{DP}$	f_{CL}	303,9	466,1	582,6	27965	Hz	
Break time (note 2)	$3/5 \times T_{DP}$	t_b	59,2	38,6	30,9	0,644	ms	M/S = H; n.c.
Make time (note 2)	$2/5 \times T_{DP}$	t_m	39,5	25,8	20,6	0,429	ms	M/S = H; n.c.
Break time (note 3)	$2/3 \times T_{DP}$	t_b	65,8	42,9	34,6	0,715	ms	M/S = L
Make time (note 3)	$1/3 \times T_{DP}$	t_m	32,9	21,5	17,2	0,358	ms	M/S = L
Inter-digit pause	$8 \times T_{DP}$	t_{id}	790	515	412	8,58	ms	
Reset delay time	$1,6 \times T_{DP}$	t_{rd}	158	103	82,4	1,72	ms	
Access pause time	$32 \times T_{DP}$	t_{ap}	3,16	2,06	1,65	0,034	s	
Prepulse duration	$1/3 \times T_{DP}$	t_d	33	21,5	17,2	0,358	ms	
Debounce time								
min	$4/30 \times T_{DP}$	$t_{e\,min}$	13,2	8,58	6,87	0,143	ms	
max.	$1/6 \times T_{DP}$	$t_{e\,max}$	16,5	10,7	8,58	0,179	ms	
Clock start-up time		$t_{on\,typ}$	4	—	—	—	ms	CE: $V_{SS} \rightarrow V_{DD}$ (note 5)
Initial data entry time (typ.)	$t_{on} + t_e$	t_i	18	14	12	4	ms	

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. Mark-to-space ratio: 3:2.
3. Mark-to-space ratio: 2:1.
4. In the n.c. (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/pull-down current.
5. Stray capacitance between pins 8 and 9: < 3 pF.

TYPICAL CURVES

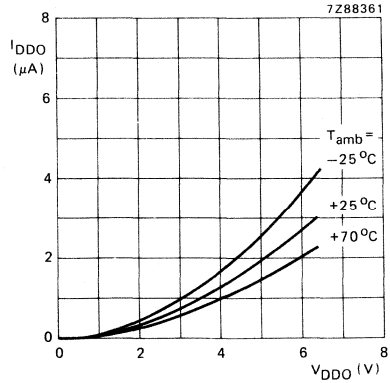


Fig. 11 Standby supply current as a function of standby supply voltage.

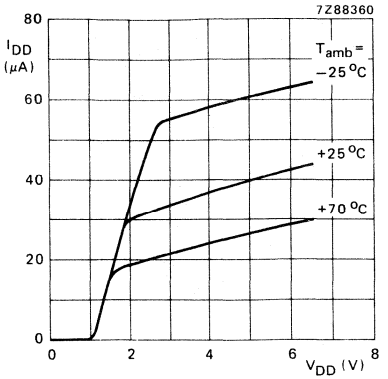


Fig. 12 Operating supply current as a function of operating supply voltage.

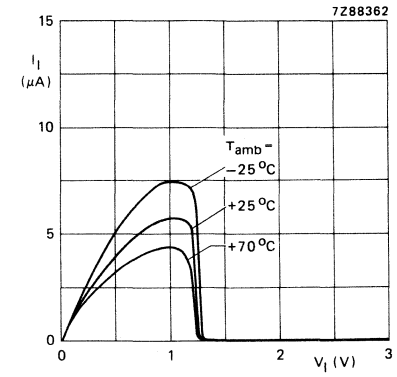


Fig. 13 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

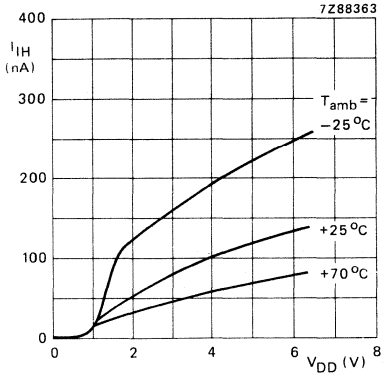


Fig. 14 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

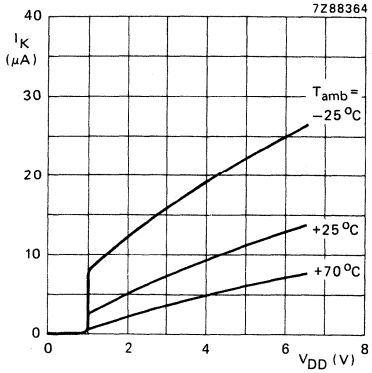


Fig. 15 Keyboard current as a function of supply voltage; X-pins connected to Y-pins.

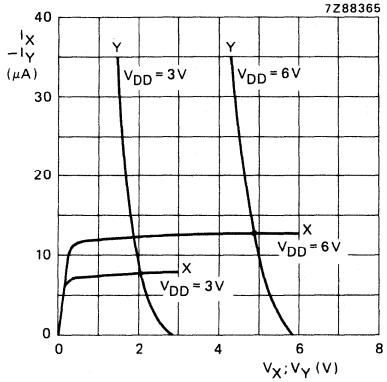


Fig. 16 Keyboard input characteristics at T_{amb} = 25 °C.

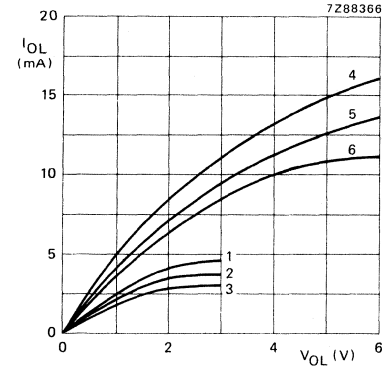


Fig. 17 Output (N-channel) sink characteristics for M1 and DP.

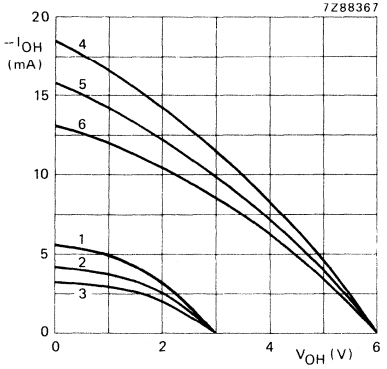


Fig. 18 Output (P-channel) source characteristics for M1 and DP.

Curves for Figs 17 and 18

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3325A is a single chip silicon-gate C-MOS integrated circuit. It converts pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The PCD3325A can regenerate access pauses during redial. During the original entry, access pauses are stored via the keyboard. A regenerated access pause can be terminated during redial in two ways: via the keyboard, or with an external dial tone recogniser circuit. This makes the circuit very suitable for redial in PABX (Private Automatic Branch Exchange) systems. The PCD3325A is pin to pin compatible with the DF320 and the MT4320 (however, including additional functions).

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- 23-digit capacity, including access pauses, for redial operation.
- Memory overflow possibility (with internally disabled redial).
- Selectable dialling pulse frequency: 10 Hz, 16 Hz and 20 Hz.
- Test pulse frequency: 932 Hz.
- Selectable dialling pulse mark/space ratios; 2 : 1 or 3 : 2.
- Hold facility for lengthening the inter-digit period.
- Circuit reset for line power breaks; $>$ 160 ms (10 Hz dialling pulse frequency).
- Access pause generation via the keyboard.
- Access pause reset:
  via the keyboard,
  with external tone recogniser.
- All inputs with pull-up/pull-down (except CE).
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102G).

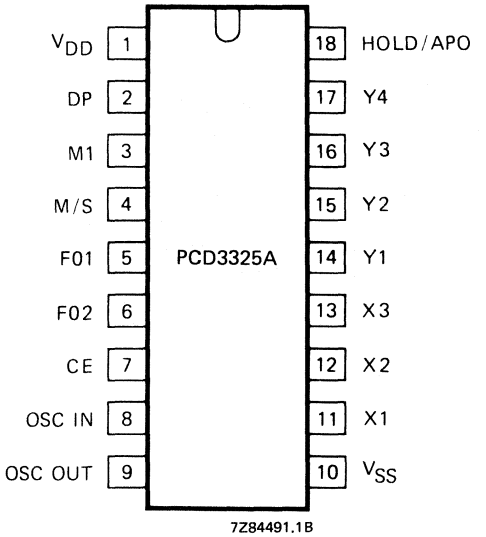


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

4	M/S	controls the mark-to-space ratio of the line pulses
5	F01	the dialling pulse frequency is defined by the logic state of these two inputs
6	F02	
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks
11	X1	column keyboard inputs with pull-down on chip
12	X2	
13	X3	
14	Y1	row keyboard inputs with pull-up on chip
15	Y2	
16	Y3	
17	Y4	

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	M1	Muting; normally used for muting during the dialling sequence

Input/output

18 HOLD/APO This pin will go HIGH when an access pause code is read from the memory during pulsing and will interrupt dialling. It can also be externally controlled; it will interrupt dialling after completion of the current digit or immediately during an inter-digit pause (t_{id}); further keyboard data will be accepted.

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

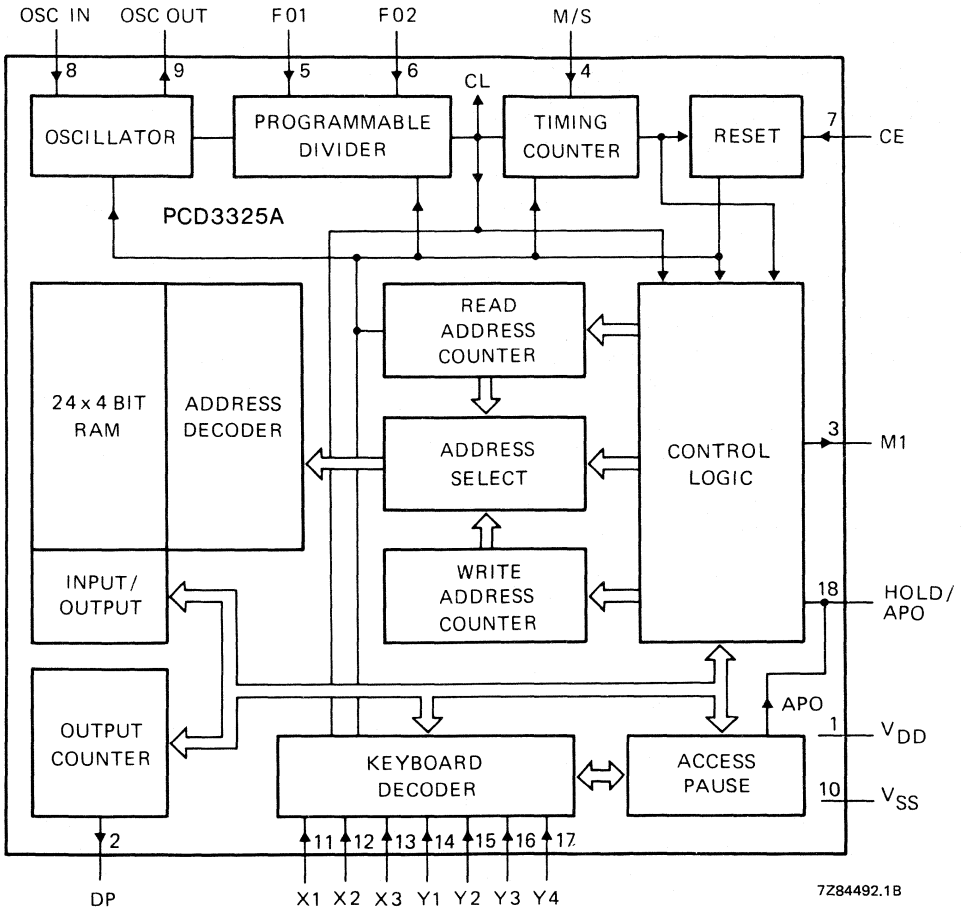


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the PCD3325A is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set (F01 and F02) to provide one of four chip system clocks; three 'normal' clock frequencies and one higher test frequency.

Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

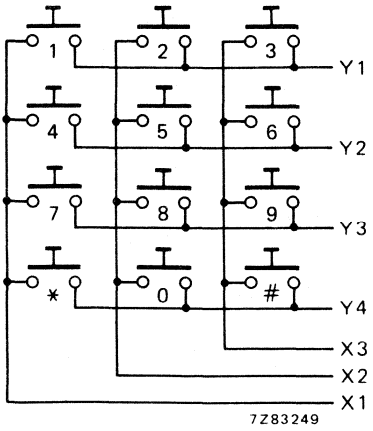
Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycodes replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the PCD3325A. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.



* Access pause set.

\# Redial or Access Pause Reset.

Fig. 3 Single contact keyboard.

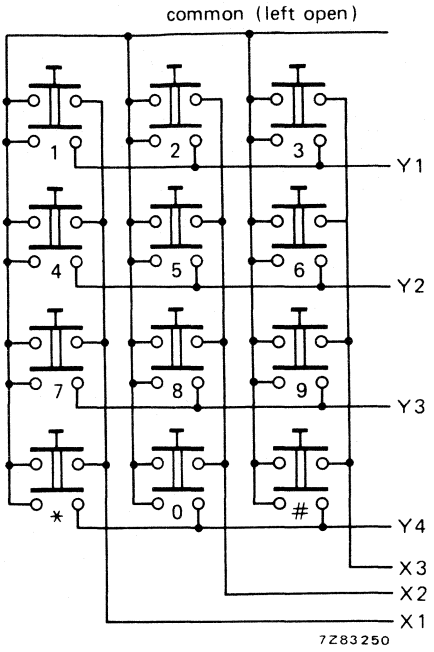


Fig. 4 Double contact keyboard.

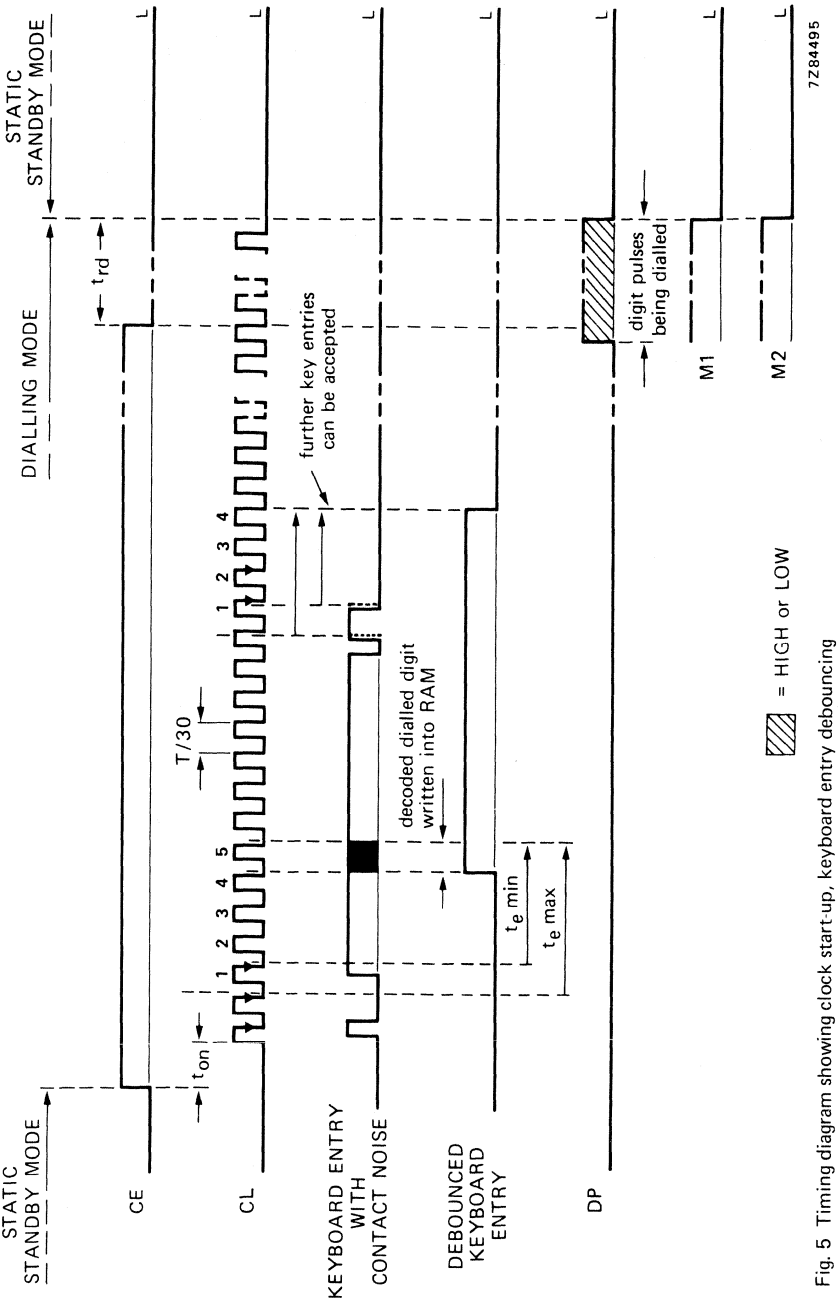


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.
N.B.: CL and M2 are internal signals.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at output M1. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

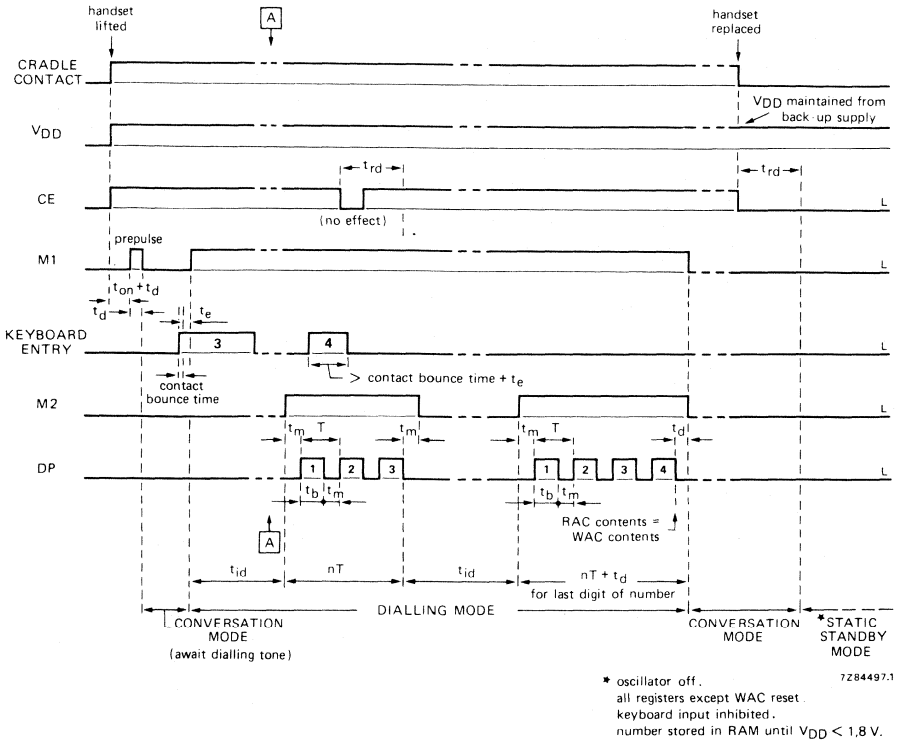


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.

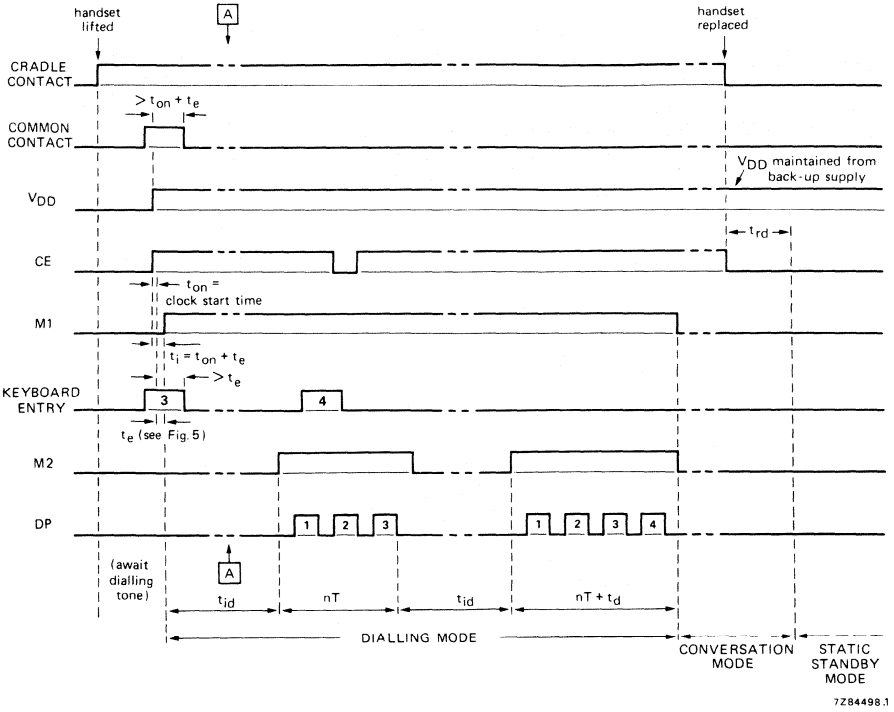


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A. M2 is an internal signal.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD/APO is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on DP until the HOLD/APO is set LOW again and an inter-digit pause has elapsed.

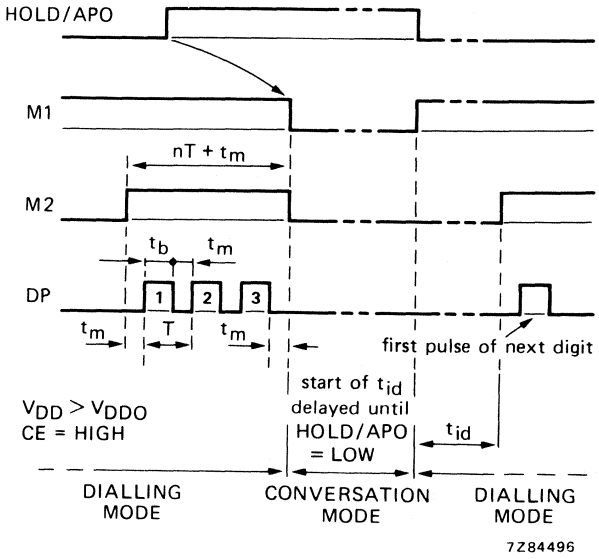


Fig. 8 Timing diagram showing the effect of activating the HOLD/APO during the transmission of dialling pulses. M2 is an internal signal.

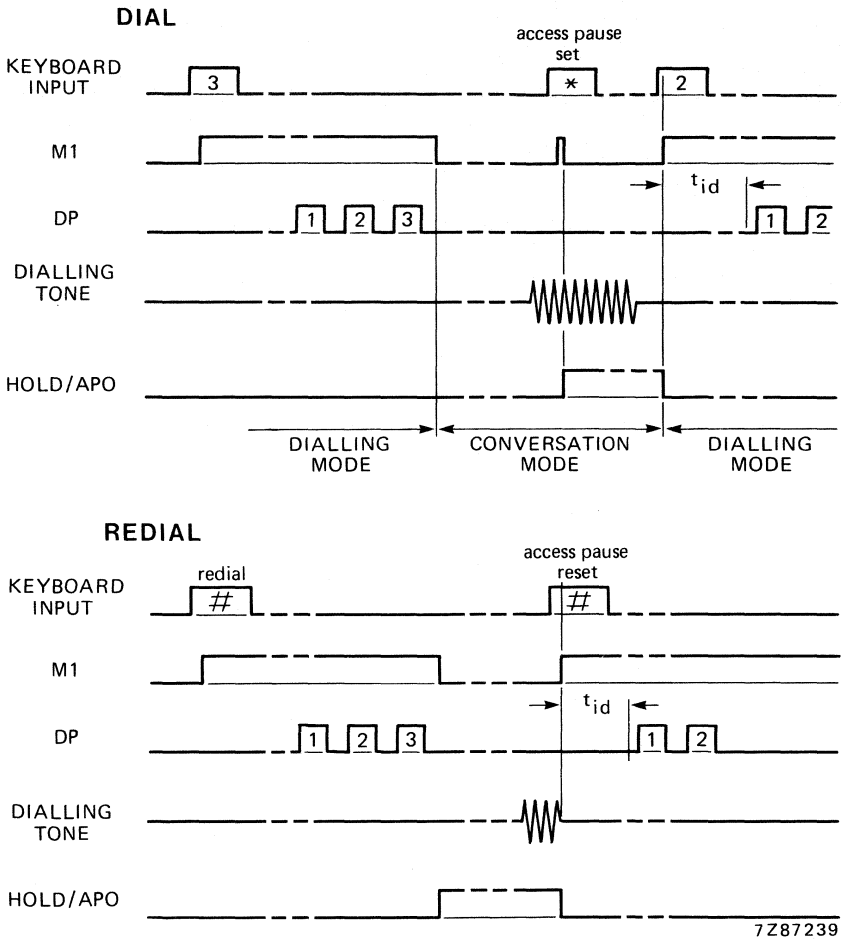


Fig. 9 Dialling sequence showing how an access pause code is stored in the RAM (DIAL) and how the access pause code is reset during the REDIAL.

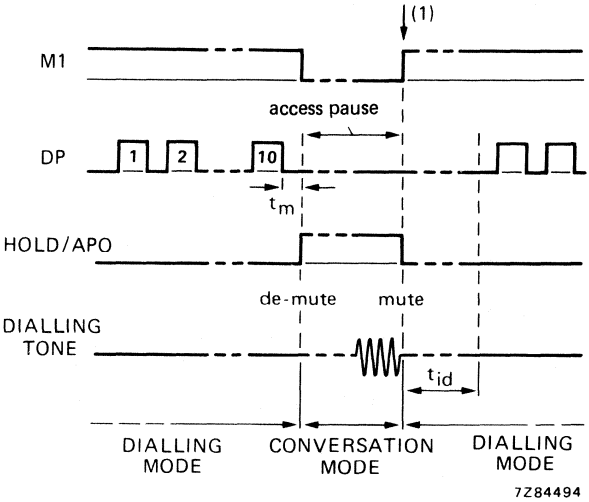
Note: access pause can be reset by pressing any key.

Access pause regeneration during redial

During original entry, access pause codes can be stored at the appropriate positions in the RAM. During redial the Access Pause Output (HOLD/APO) will go HIGH as soon as an access pause code is read from the RAM, thereby interrupting dialling until HOLD/APO is made LOW again as described above. In this way the normal inter-digit pause with a duration t_{id} can be replaced by a proper access pause. An access pause code is stored in the RAM during original entry by pressing the access pause key (*) between entering the trunk exchange code and the subscriber code, or at any other moment an access pause is required. The number of access pauses that can be inserted in this manner is only limited by the capacity of the RAM (digits + access pauses $\leqslant$ 23).

During redial, access pauses will be automatically regenerated.
Two methods of terminating an access pause:

1. Manually, by pressing the redial key (#)
2. With an external tone recogniser, by forcing HOLD/APO to LOW.



(1) a. Access pause reset by pressing redial key (#).
b. HOLD/APO controlled by tone recogniser:
HOLD/APO forced to LOW.

Fig. 10 Timing diagram showing Access Pause Reset, during redial.

Note: access pause can be reset by pressing any key.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS}−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified.

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	T_{amb} = −25 to +70 °C
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to +70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = V_{DD}; notes 2, 3
	I_{DD}	–	50	100	μA	CE = V_{DD}; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	5	μA	CE = V_{SS} ; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V; T_{amb} = −25 to +70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		1,8 V ⩽ V_{DD} ⩽ 6 V
Input leakage current; CE LOW	$-I_{IL}$	–	–	50	nA	CE = V_{SS}
HIGH	I_{IH}	–	–	50	nA	CE = V_{DD}
Pull-up input current M/S	$-I_{IL}$	30	100	300	nA	V_I = V_{SS}
Pull-down input current F01, F02	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	V_I = V_{SS}

DEVELOPMENT SAMPLE DATA

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 8 and 9 < 3 pF.
4. Guarantees correct keyboard operation.

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.		conditions
Outputs M1, DP						
sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V
Latch output HOLD/APO						
sink current	I_{OL}	50	130	300	μA	V_{OL} = 0,5 V
source current	$-I_{OH}$	45	110	250	μA	V_{OH} = 2,5 V

TIMING DATA

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

input levels of F01 and F02 (V_{SS} = LOW; V_{DD} = HIGH)		V_{F01}	LOW	HIGH	LOW	HIGH		
		V_{F02}	LOW	HIGH	HIGH	LOW		conditions (note 4)
		symbol				(test mode)		
Dialling pulse frequency	$1/T_{DP}$	f_{DP}	10,13	15,54	19,42	939,2	Hz	note 1
Dialling pulse period	$1/f_{DP}$	T_{DP}	98,7	64,4	51,5	1,073	ms	
Clock pulse frequency	$30 \times f_{DP}$	f_{CL}	303,9	466,1	582,6	27965	Hz	
Break time (note 2)	$3/5 \times T_{DP}$	t_b	59,2	38,6	30,9	0,644	ms	M/S = H; n.c.
Make time (note 2)	$2/5 \times T_{DP}$	t_m	39,5	25,8	20,6	0,429	ms	M/S = H; n.c.
Break time (note 3)	$2/3 \times T_{DP}$	t_b	65,8	42,9	34,6	0,715	ms	M/S = L
Make time (note 3)	$1/3 \times T_{DP}$	t_m	32,9	21,5	17,2	0,358	ms	M/S = L
Inter-digit pause	$8 \times T_{DP}$	t_{id}	790	515	412	8,58	ms	
Reset delay time	$1,6 \times T_{DP}$	t_{rd}	158	103	82,4	1,72	ms	
Prepulse duration	$1/3 \times T_{DP}$	t_d	33	21,5	17,2	0,358	ms	
Debounce time								
min	$4/30 \times T_{DP}$	$t_{e\,min}$	13,2	8,58	6,87	0,143	ms	
max.	$1/6 \times T_{DP}$	$t_{e\,max}$	16,5	10,7	8,58	0,179	ms	
Clock start-up time		$t_{on\,typ}$	4	–	–	–	ms	CE: $V_{SS} \rightarrow V_{DD}$ (note 5)
Initial data entry time (typ.)	$t_{on} + t_e$	t_i	18	14	12	4	ms	

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. Mark-to-space ratio: 3:2.
3. Mark-to-space ratio: 2:1.
4. In the n.c. (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/pull-down current.
5. Stray capacitance between pins 8 and 9: < 3 pF.

TYPICAL CURVES

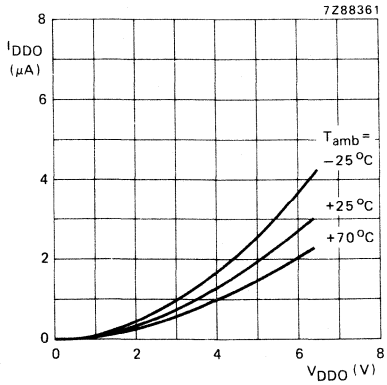


Fig. 11 Standby supply current as a function of standby supply voltage.

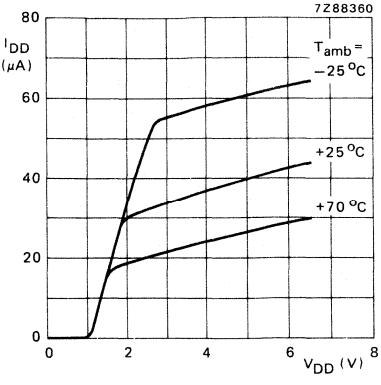


Fig. 12 Operating supply current as a function of operating supply voltage.

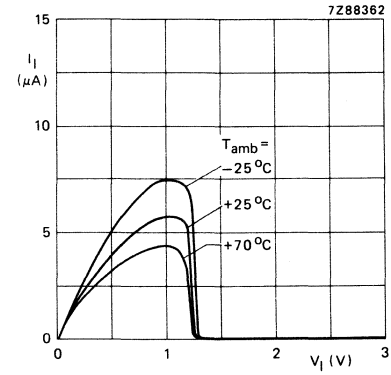


Fig. 13 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

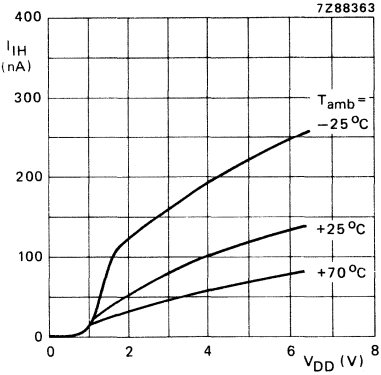


Fig. 14 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

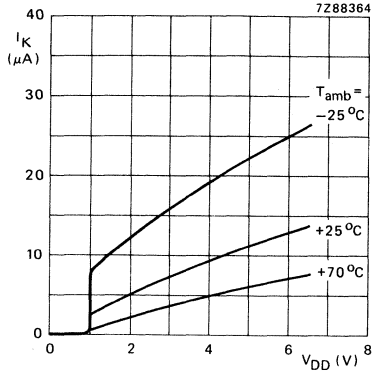


Fig. 15 Keyboard current as a function of supply voltage;
X-pins connected to Y-pins.

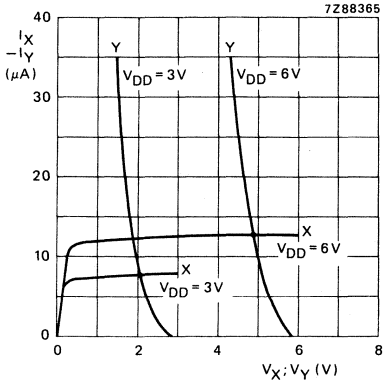


Fig. 16 Keyboard input characteristics at T_{amb} = 25 °C.

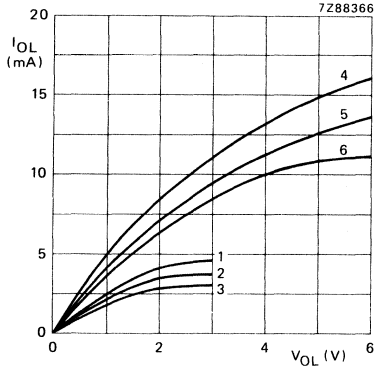


Fig. 17 Output (N-channel) sink characteristics for M1 and DP.

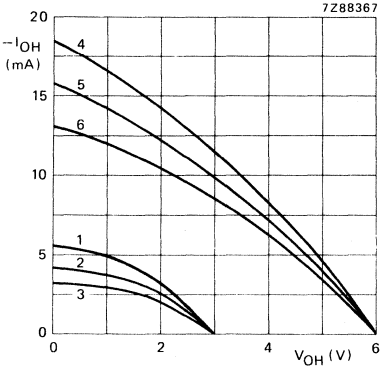


Fig. 18 Output (P-channel) source characteristics for M1 and DP.

Curves for Figs 17 and 18

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3326 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The PCD3326 can regenerate access pauses during redial. During the original entry, access pauses are stored either automatically or via the keyboard. A regenerated access pause can be terminated during redial in three ways: automatically after a built-in time, or via the keyboard, or with an external dial tone recogniser circuit. This makes the circuit very suitable for redial in PABX (Private Automatic Branch Exchange) systems.

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- 23-digit capacity, including access pauses, for redial operation.
- Memory overflow possibility (with internally disabled redial).
- Selectable dialling pulse frequency: 10 kHz, 16 Hz and 20 Hz.
- Test pulse frequency: 932 Hz.
- Hold facility for lengthening the inter-digit period.
- Circuit reset for line power breaks; $>$ 160 ms (10 Hz dialling pulse frequency).
- Access pause generation automatically or via the keyboard.
- Access pause reset:
  automatically after 3 s or 6 s (10 Hz dialling pulse frequency),
  via the keyboard,
  with external tone recogniser.
- All inputs with pull-up/pull-down (except CE)
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINES

PCD3326P: 18-lead DIL; plastic (SOT-102G).

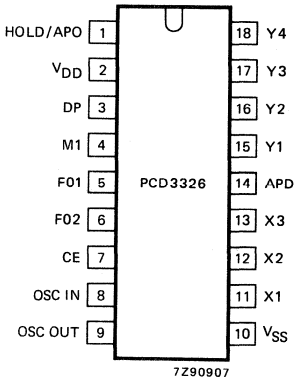


Fig. 1 Pinning diagram.

PINNING

2	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

5	F01	the dialling pulse frequency is defined by the logic state of these two inputs
6	F02	
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks
11	X1	column keyboard inputs with pull-down on chip
12	X2	
13	X3	
14	APD	Access Pause Delay; selects the maximum duration of an access pause.
15	Y1	row keyboard inputs with pull-up on chip
16	Y2	
17	Y3	
18	Y4	

Outputs

3	DP	Dialling Pulse; drive of the external line switching transistor or relay
4	M1	Muting; normally used for muting during the dialling sequence

Input/output

1 HOLD/APO This pin will go HIGH when an access pasue code is read from the memory during pulsing and will interrupt dialling. It can also be externally controlled; it will interrupt dialling after completion of the current digit or immediately during an inter-digit pause (t_{id}); further keyboard data will be accepted.

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

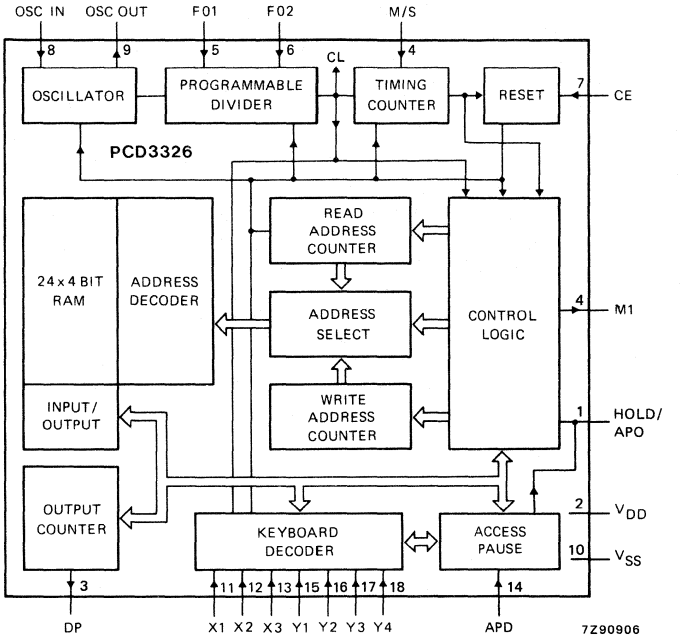


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the PCD3326 is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set (F01 and F02) to provide one of four chip system clocks; three 'normal' clock frequencies and one higher test frequency.

Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = V_{SS} provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = V_{DD} the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

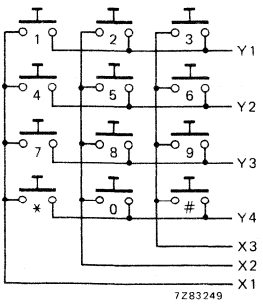
Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the PCD3326. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.



★ Access pause set.

Redial or Access Pause Reset.

Fig. 3 Single contact keyboard.

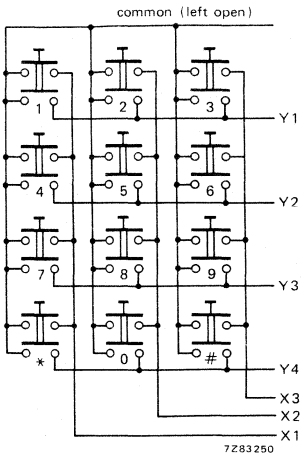


Fig. 4 Double contact keyboard.

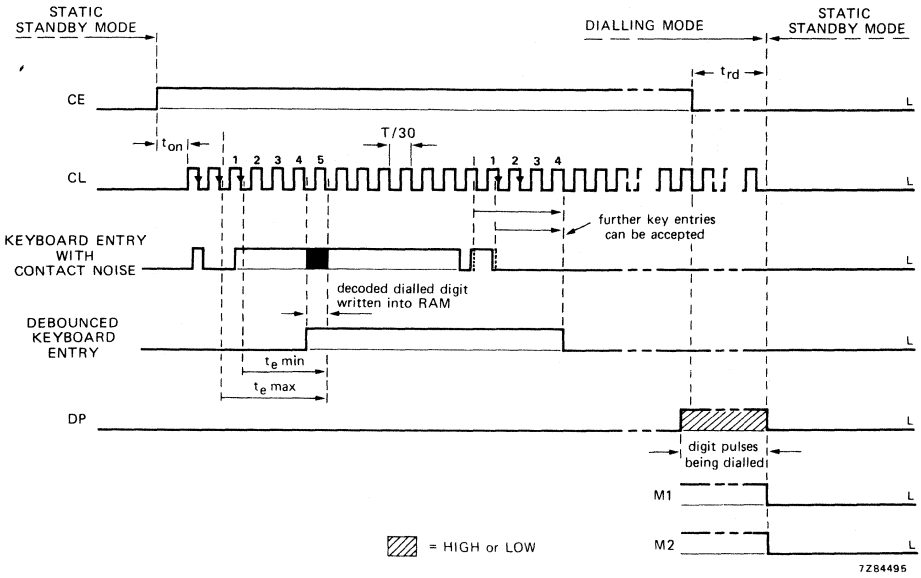


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling.

N.B.: CL and M2 are internal signals.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at output M1. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

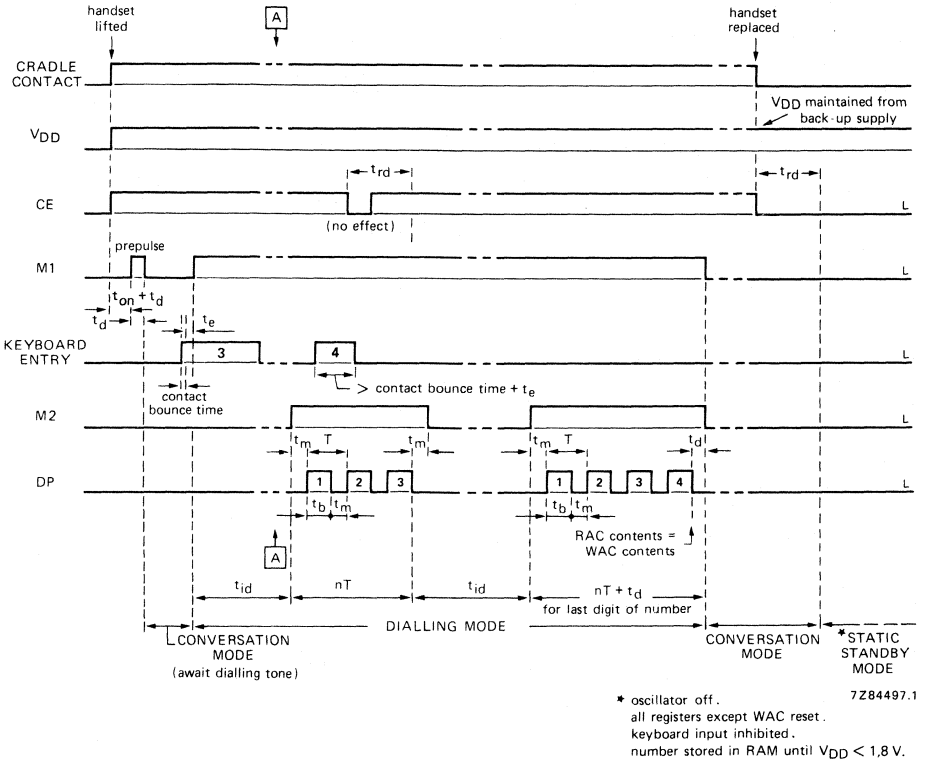


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.

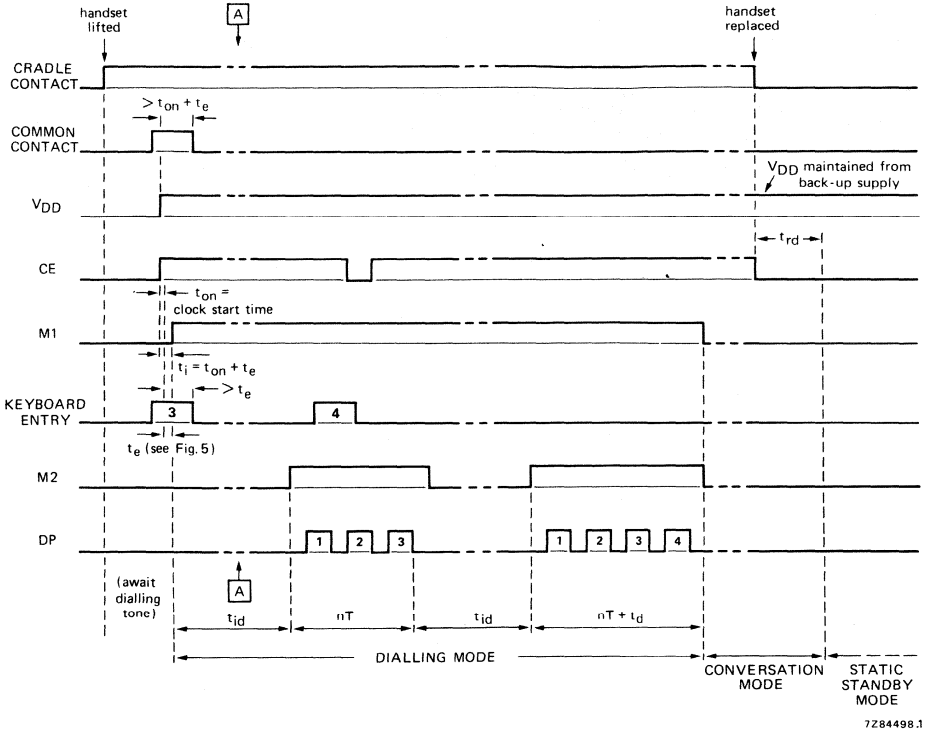


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A. M2 is an initial signal.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD/APO is set HIGH, the dialling pulse train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in the RAM. No further keycodes will be read from the RAM and converted into dialling pulses on DP until the HOLD/APO is set LOW again and an inter-digit pause has elapsed.

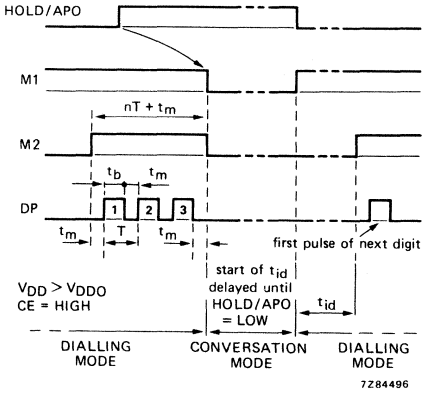


Fig. 8 Timing diagram showing the effect of activating the HOLD/APO during the transmission of dialling pulses. M2 is an internal signal.

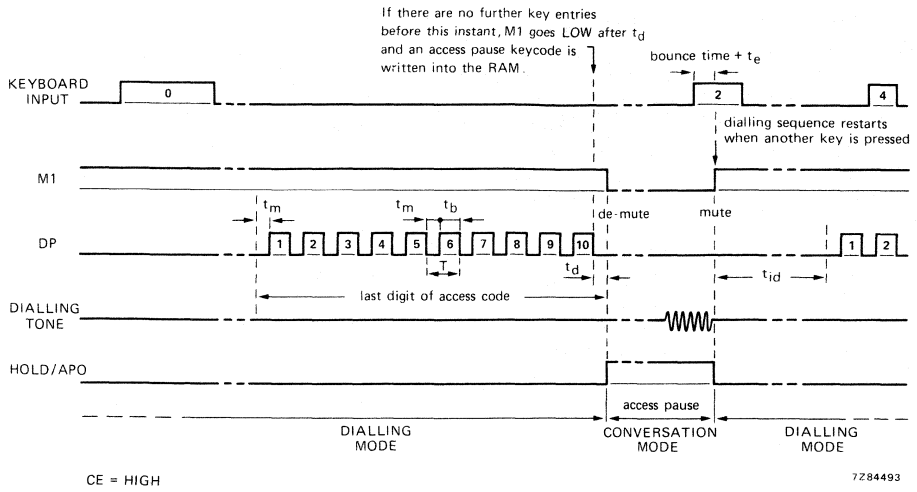


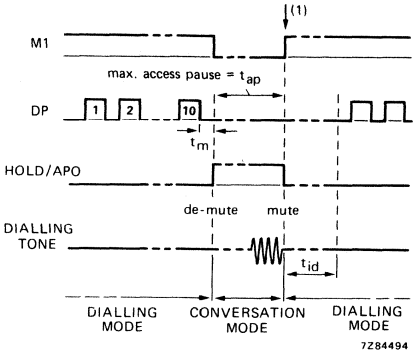
Fig. 9 Dialling sequence showing how an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.

Access pause regeneration during redial

During original entry, access pause codes can be stored at the appropriate positions in the RAM. During redial the Access Pause Output (HOLD/APO)will go HIGH as soon as an access pause code is read from the RAM, thereby interrupting dialling until HOLD/APO is made LOW again as described above. In this way the normal inter-digit pause with a duration t_{id} can be replaced by a proper access pause. An access pause code is now automatically stored in the RAM during original entry, when M1 goes LOW, after all digits so far entered have been transmitted (see Fig. 6). This occurs between entering of the trunk exchange code and the subscriber code, whilst the access tone is available. Up to two access pauses can be entered into the RAM in this manner. Alternatively, the access pause key (★) can still be pressed to insert (more) access pauses manually (digits + access pauses $\leqslant 23$).
During redial, access pauses will be automatically regenerated.

Three methods of terminating an access pause:

1. Automatically, if the built-in time t_{ap} expires; HOLD/APO then goes LOW; tap can be set to one of two values with the Access Pause Delay (APD) select input.
2. Manually, by pressing the redial key before t_{ap} expires.
3. With an external tone recogniser, by forcing HOLD/APO to LOW or HIGH respectively, for shortening or lengthening an access pause.



(1) a. Access pause (t_{ap}) expires or press redial before end of t_{ap}.

b. HOLD/APO controlled by tone recogniser:
HOLD/APO forced to LOW before t_{ap} expires; access pause $< t_{ap}$
HOLD/APO forced to HIGH after t_{ap} expires; access pause $> t_{ap}$.

Fig. 10 Timing diagram showing Access Pause Reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS} −0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified.

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to +70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = V_{DD}; notes 2, 3
	I_{DD}	–	50	100	μA	CE = V_{DD}; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	2	μA	CE = V_{SS}; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V T_{amb} = −25 to +70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		
Input leakage current; CE						
LOW	$-I_{IL}$	–	–	50	nA	CE = V_{SS}
HIGH	I_{IH}	–	–	50	nA	CE = V_{DD}
Pull-up input current M/S	$-I_{IL}$	30	100	300	nA	V_I = V_{SS}
Pull-down input current F01, F02, APD	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = V_{DD}
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	V_I = V_{SS}

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 8 and 9 < 3 pF.
4. Guarantees correct keyboard operation.

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.		conditions
Outputs M1, DP						
sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V
Latch output HOLD/APO						
sink current	I_{OL}	50	130	300	μA	V_{OL} = 0,5 V
source current	$-I_{OH}$	45	110	250	μA	V_{OH} = 2,5 V

TIMING DATA

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 0 V; f_{osc} = 3,579545 MHz

input levels of F01 and F02		V_{F01}	LOW	HIGH	LOW	HIGH		
(V_{SS} = LOW; V_{DD} = HIGH)		V_{F02}	LOW	HIGH	HIGH	LOW		conditions (note 3)
		symbol				(test mode)		
Dialling pulse frequency	$1/T_{DP}$	f_{DP}	10,13	15,54	19,42	939,2	Hz	note 1
Dialling pulse period	$1/f_{DP}$	T_{DP}	98,7	64,4	51,5	1,073	ms	
Clock pulse frequency	$30 \times f_{DP}$	f_{CL}	303,9	466,1	582,6	27965	Hz	
Break time (note 2)	$3/5 \times T_{DP}$	t_b	59,2	38,6	30,9	0,644	ms	M/S = H; n.c.
Make time (note 2)	$2/5 \times T_{DP}$	t_m	39,5	25,8	20,6	0,429	ms	M/S = H; n.c.
Inter-digit pause	$8 \times T_{DP}$	t_{id}	790	515	412	8,58	ms	
Reset delay time	$1,6 \times T_{DP}$	t_{rd}	158	103	82,4	1,72	ms	
Access pause time	$32 \times T_{DP}$	t_{ap}	3,16	2,06	1,65	0,034	s	ADP = L; nc
	$64 \times T_{DP}$	t_{ap}	6,32	4,12	3,30	0,069	s	ADP = H
Prepulse duration	$1/3 \times T_{DP}$	t_d	33	21,5	17,2	0,358	ms	
Debounce time								
min.	$4/30 \times T_{DP}$	$t_{e\,min}$	13,2	8,58	6,87	0,143	ms	
max.	$1/6 \times T_{DP}$	$t_{e\,max}$	16,5	10,7	8,58	0,179	ms	
Clock start-up time		$t_{on\,typ}$	4	4	4	4	ms	CE: $V_{SS} \rightarrow V_{DD}$ (note 4)
Initial data entry time (typ.)	$t_{on} + t_e$	t_i	18	14	12	4	ms	

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. Mark-to-space ratio: 3:2.
3. In the n.c. (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/pull-down current.
4. Stray capacitance between pins 8 and 9: < 3 pF.

TYPICAL CURVES

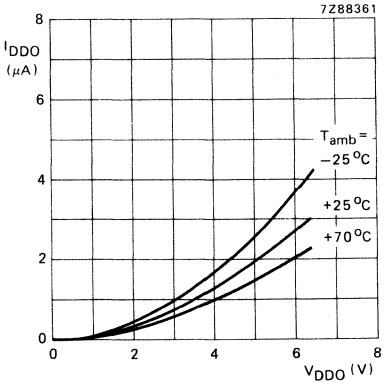


Fig. 11 Standby supply current as a function of standby supply voltage.

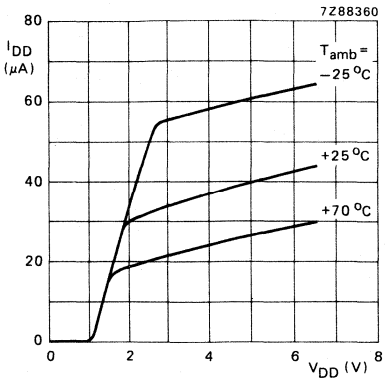


Fig. 12 Operating supply current as a function of operating supply voltage.

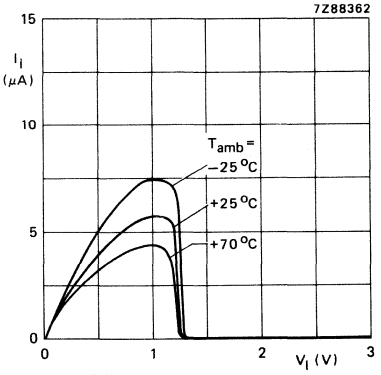


Fig. 13 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

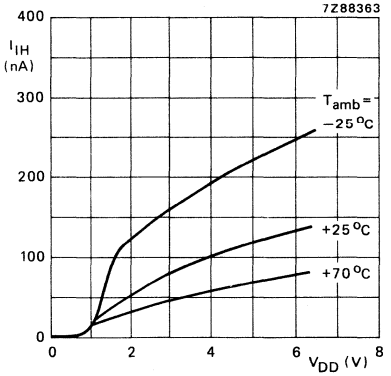


Fig. 14 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

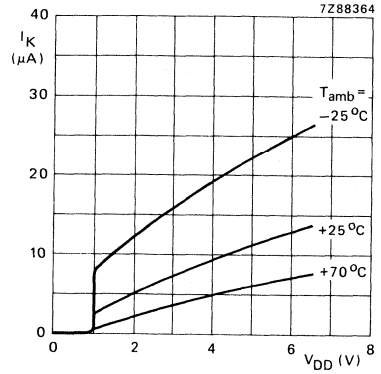


Fig. 15 Keyboard current as a function of supply voltage; X-pins connected to Y-pins.

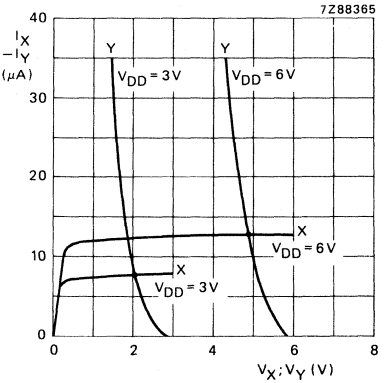


Fig. 16 Keyboard input characteristics at T_{amb} = 25 °C.

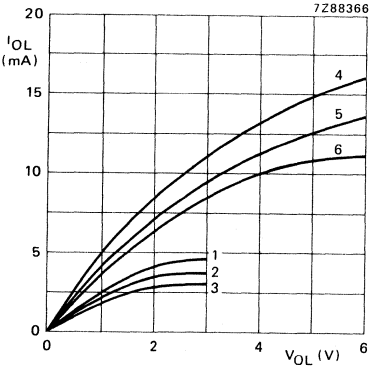


Fig. 17 Output (N-channel) sink characteristics for M1 and DP.

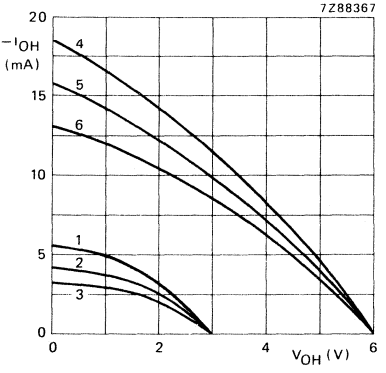


Fig. 18 Output (P-channel) source characteristics for M1 and DP.

Curves for Figs 17 and 18

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

CMOS MICROCONTROLLER FOR TELEPHONE SETS

GENERAL DESCRIPTION

The PCD3343 is a single-chip 8-bit microcontroller fabricated in CMOS and is a member of the PCF8500 family. It has special on-chip features for application in telephone sets.
The device is mask programmable, designed to provide telephone dialling facilities such as redial, repertory dial, emergency call, keyboard scan and control for liquid crystal display, pulse dial and/or DTMF dial via dedicated peripheral.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 3 K ROM bytes
- 224 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- Serial I/O which can be used in bus systems with more than one master (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048, MAB8400 and PCF8500)
- All instructions 1 or 2 cycles
- Clock frequency 100 kHz to 10 MHz
- Single supply voltage from 1,8 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator with output drive capability for peripherals (e.g. PCD3312 DTMF generator)
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3343P: 28-lead DIL; plastic (SOT-117D).
PCD3343D: 28-lead DIL; ceramic (CERDIP) (SOT-135A).
PCD3343T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

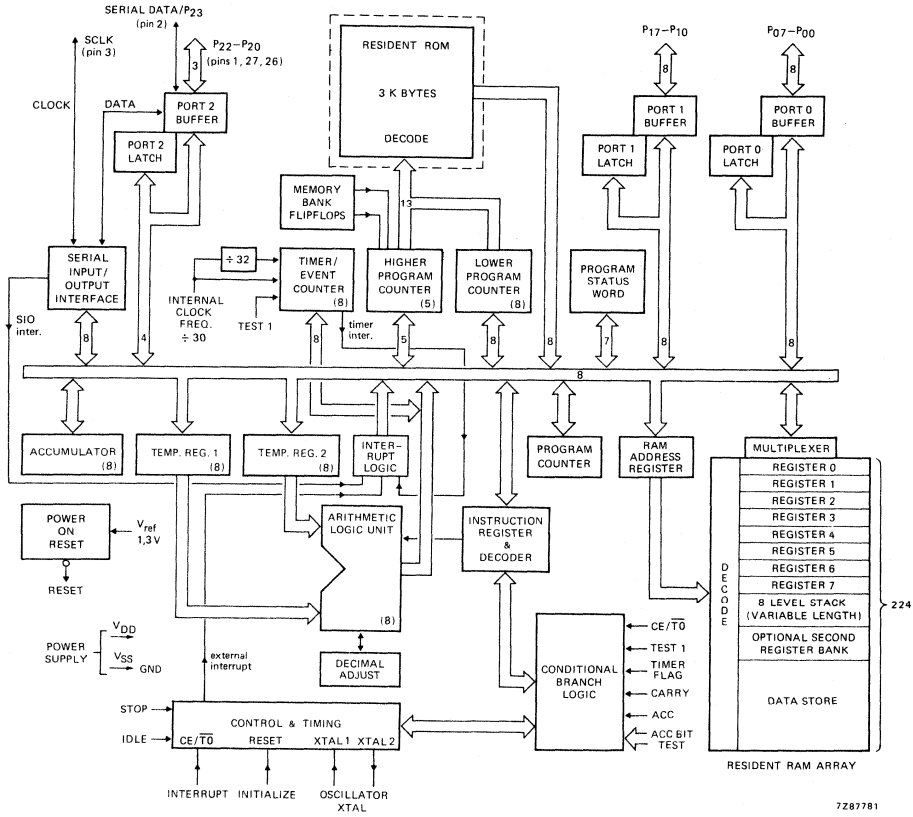
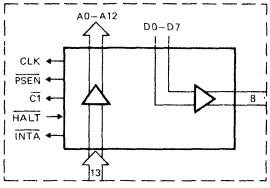
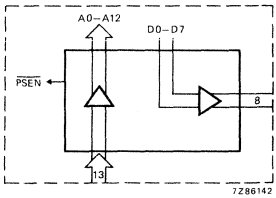


Fig. 1 Block diagram; PCD3343.



(a)

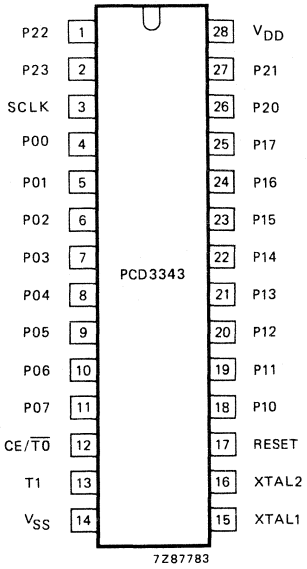
Fig. 1a Replacement of dotted part in Fig. 1, for the PCF8500F bond-out version.



(b)

Fig. 1b Replacement of dotted part in Fig. 1, for the PCF8500B 'Piggy-back' version.

PINNING



Note CE/$\overline{T0}$ is labelled $\overline{INT}$/T0 on the PCF8500B and has inverted polarity.

Fig. 2 Pinning diagram: PCD3343 and bottom pinning PCF8500B.

PIN DESIGNATION

3	SCLK	**Clock**: bidirectional clock for serial I/O.
4-11	P00-P07	**Port 0**: 8-bit quasi-bidirectional I/O port.
12	CE/$\overline{T0}$	**Interrupt/Test 0**: external interrupt input (sensitive to positive-going edge)/test input pin; when used as a test input directly tested by conditional branch instructions JT0 and JNT0.
13	T1	**Test 1**: test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
14	V_{SS}	**Ground**: circuit earth potential.
15	XTAL 1	**Crystal input**: connection to timing component (crystal) which determines the frequency of the internal oscillator; also the input for an external clock source.
16	XTAL 2	connection to the other side of the timing component.
17	RESET	**Reset input**: used to initialize the processor (active HIGH), or output of power-on-reset circuit.
18-25	P10-P17	**Port 1**: 8-bit quasi-bidirectional I/O port.
26, 27, 1, 2	P20-P23	**Port 2**: 4-bit quasi-bidirectional I/O port. P23 is the serial data input/output in serial I/O mode.
28	V_{DD}	**Power supply**: 1,8 V to 6 V.

PINNING (continued)

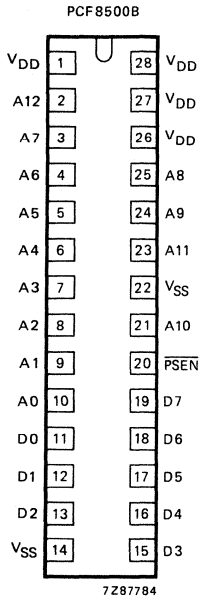


Fig. 3 Pinning diagram: PCF8500B 'Piggy-back' version top pinning; to access a 2732 or 2764 EPROM.

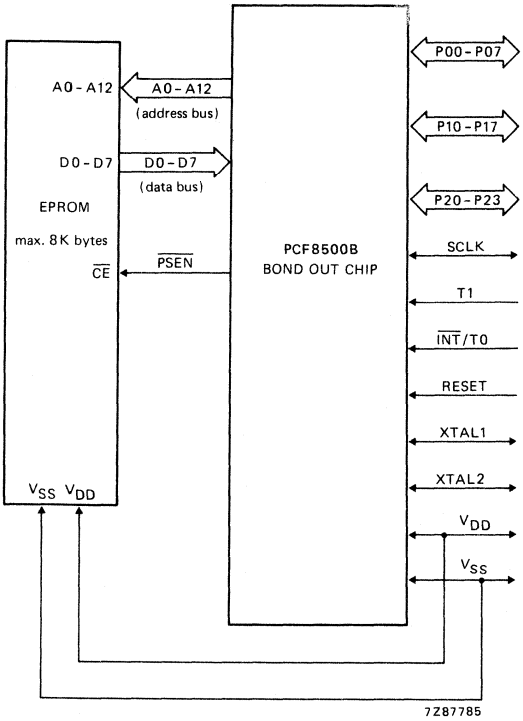


Fig. 3a Connection of EPROM to 'Piggy-back' package PCF8500B.

PIN DESIGNATION

14, 22	V_{SS}	**Ground**
1, 26-28	V_{DD}	**Power supply**
10-3, 25, 24, 21, 23, 2	A0-A12	**Address outputs**
11-13, 15-19	D0-D7	**Data**
20	$\overline{PSEN}$	**Program store enable**

Notes

1. RAM capacity of PCF8500B is 256 bytes.
2. Access time for ROMS/EPROMS to be below 7 x $1/f_{XTAL}$.
3. Pin 12 CE/$\overline{T0}$ is on the PCF8500B, inverted and labelled $\overline{INT}$/T0.

FUNCTIONAL DESCRIPTION

Bond-out version PCF8500F

The PCF8500F is a microcontroller that contains no on-board ROM, but has all address and data lines brought-out to access an external ROM or EPROM. This version has more pins than the PCD3343 with on-board ROM (see Fig. 1a). The RAM has 256 bytes. It can address 8 K bytes of ROM.

'Piggy-back' version PCF8500B

The PCF8500B is a special package that has standard pinning to the bottom which facilitates insertion as a mask-programmed device. An EPROM can be mounted on top in an additional socket. The total package height is greater than the standard DIL package. The RAM has 256 bytes and can also address 8 K bytes of program memory.

Program memory PCD3343

The program memory consists of 3072 bytes (8-bit words), in a read-only memory (ROM). Each location is directly addressable by the program counter. The memory is mask-programmed at the factory. Figure 4 shows the program memory map.

Four program memory locations are of special importance:

- Location 0; contains the first instruction to be executed after the processor is initialized (RESET),
- Location 3; contains the first byte of an external interrupt service subroutine,
- Location 5; contains the first byte of a serial I/O interrupt service subroutine,
- Location 7; contains the first byte of a timer/event counter interrupt service subroutine.

Program memory is arranged in banks of 2 K bytes, which are selected by SEL MB instructions. The program memory is further divided into location 'pages', each of 256 bytes. This latter division applies only for conditional branches. Memory bank boundaries can be crossed only by using the unconditional branch instructions after the appropriate memory bank has been selected. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data memory PCD3343

Data memory consists of 224 bytes (8-bit words), random-access data memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 5 shows the data memory map.

Working registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service subroutines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

FUNCTIONAL DESCRIPTION (continued)

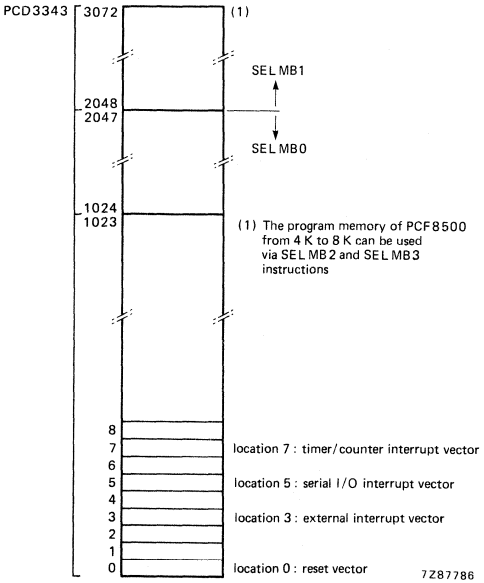


Fig. 4 Program memory map.

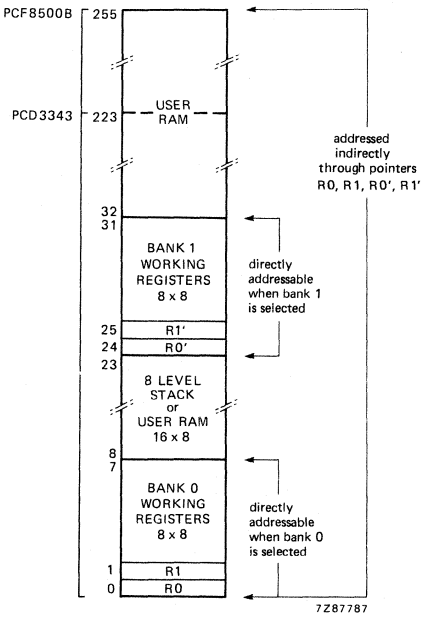


Fig. 5 Data memory map.

Program counter stack

Locations 8 to 23 may be designated as an 8-level program counter stack (2 locations per level), or as general purpose RAM. The program counter stack (Fig. 6) enables the processor to keep track of the return addresses and status generated by interrupts or CALL instructions by storing the contents of the program counter prior to servicing the subroutine. A 3-bit stack pointer determines which of the eight register pairs of the program counter stack will be loaded with next generated return address.

The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the program counter and bits 4, 6 and 7 of the program status word (PSW) are transferred to locations 8 and 9. The stack pointer increments by one and points to locations 10 and 11 ready for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the stack pointer decrements by one and the contents of the register pair on top of the stack are transferred to the program counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If not all 8 levels of subroutine and interrupt nesting are used, the unused portion of the stack may be used as any other indirectly addressable RAM locations. Possible locations from 32 to 223 may be used for storage of program variables or data.

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

The value of the saved contents of the program counter is different for an interrupt CALL compared to a normal CALL to subroutine. With an interrupt CALL, the program counter return address is saved; with a subroutine CALL, the saved program counter value is one less than the program counter return address.

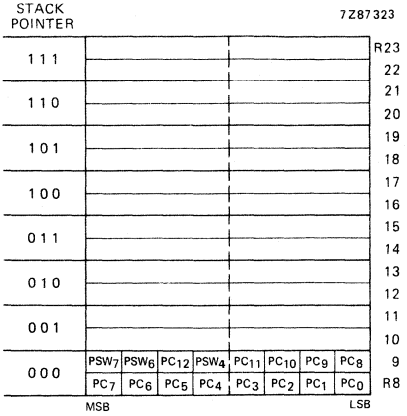


Fig. 6 Program counter stack.

IDLE and STOP modes

IDLE mode

When the microcontroller enters the IDLE mode via the IDLE instruction (H'01') the oscillator, timer/counter and serial I/O are kept running. The microcontroller exits from the IDLE mode by one of three interrupts if they are enabled or by activating a RESET. If the interrupt is not enabled the processor will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Fig. 7).

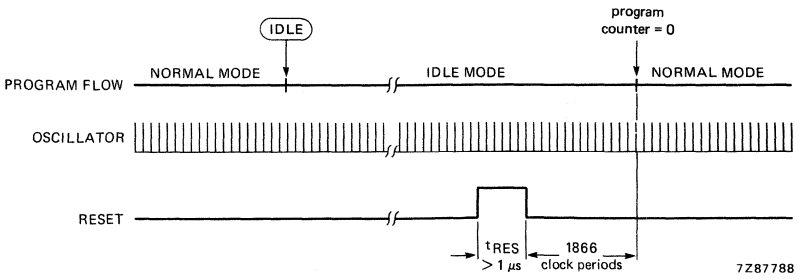


Fig. 7 Exit from IDLE mode via a RESET.

FUNCTIONAL DESCRIPTION (continued)

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out. A LOW-to-HIGH transition on the external interrupt pin (CE/$\overline{T0}$) reactivates the microcontroller. A HIGH level applied to CE/$\overline{T0}$ will reactivate the microcontroller only in the STOP mode. Thus, if CE/$\overline{T0}$ was HIGH before the microcontroller entered the IDLE mode, it must go LOW before the microcontroller can be reactivated (see Fig. 8).

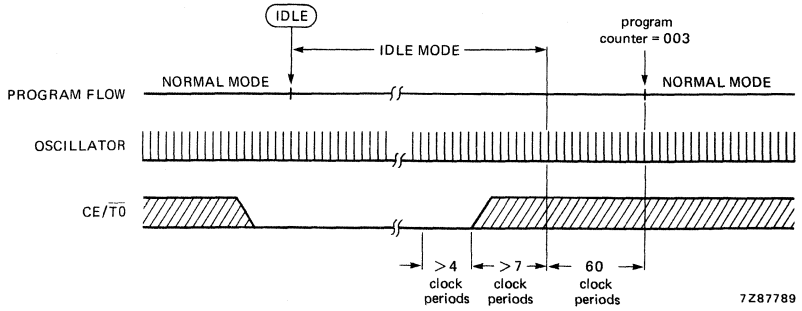


Fig. 8 Exit from IDLE mode via an interrupt.

Wake-up from the IDLE mode is ensured when CE/$\overline{T0}$ is LOW for 4 CP (clock periods) followed by a HIGH for 7 CP. After the initial forced CALL H'003' operation (60 CP) the program continues with the external interrupt service routine.

STOP mode

The microcontroller enters the STOP mode by the STOP instruction (H'22'). The oscillator is switched off. The internal status of the CPU, RAM contents and the state of I/O ports are not affected. The microcontroller can be brought-out of the STOP mode by an active signal at the external interrupt input or by an external RESET signal. When one of these two signals is applied an internal delay of 1866 CP is provided to ensure that all internal clocks are operating correctly before restart (see Fig. 9).

If the microcontroller exits from the STOP mode by activating RESET, a normal RESET sequence is executed.

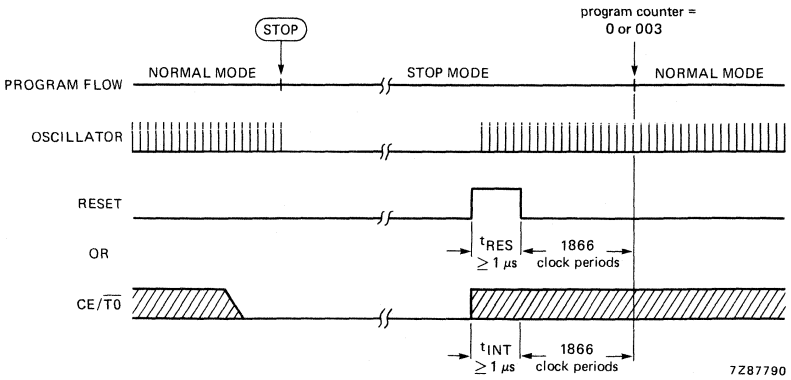


Fig. 9 Entering and exiting the STOP mode.

If the microcontroller exits the STOP mode by pulling the external interrupt input pin HIGH, an interrupt sequence is executed only if the external interrupt is enabled. In this event the microcontroller resumes the normal program sequence after returning from the interrupt routine, as in the normal mode. If the interrupt is not enabled, it continues the normal program sequence, executing the instruction following the STOP instruction.

The microcontroller is restarted by a HIGH level applied at the CE/$\overline{T0}$ pin, and not by a LOW-to-HIGH transition as in a normal interrupt mechanism.

When the CE/$\overline{T0}$ level is active during the STOP instruction then no STOP is executed.

A HIGH level on the external interrupt input of at least 1 μs will cause the microcontroller to exit the STOP mode.

I/O facilities

The PCD3343 family has 23 I/O lines arranged as:

- Port 0 parallel port of 8 lines (P00 to P07)
- Port 1 parallel port of 8 lines (P10 to P17)
- Port 2 parallel port of 4 lines (P20 to P23)
- SCLK serial I/O consisting of a data line shared with a parallel port line (P23) and a separate clock line SCLK
- CE/$\overline{T0}$ external interrupt and test input. When used as a test input can be directly tested by conditional branch instructions JT0 and JNT0
- T1 test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter.

Parallel ports

All parallel ports can be used as outputs or inputs, their structure is quasi-bidirectional.
Output data written to a port is latched and remains unchanged until rewritten.
Input data is not latched and so must be present until read by an input instruction.

Input lines are fully CMOS compatible, output lines can drive one LS-TTL or CMOS load.

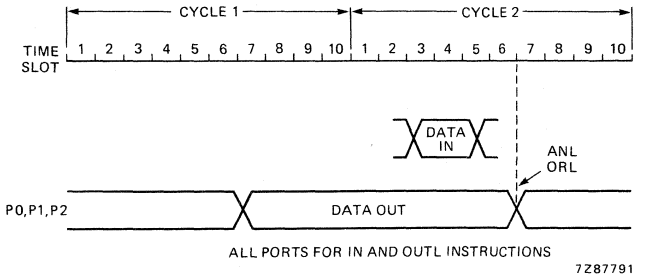


Fig. 10 Timing diagram of all ports on IN and OUTL instructions; for ANL and ORL instructions, the ports change on the time slot 7 of cycle 2.

Fig. 11 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source.
Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current provides sufficient source current for a TTL HIGH level, yet can be pulled LOW by an external CMOS device, thus allowing the same pin to be used for both input and output.

FUNCTIONAL DESCRIPTION (continued)

When a logic 1 is written to the line for the first time (MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period), to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to the port lines will not switch TR2 on. This prevents unnecessary current through external components connected to the port lines of the same port which might be in the input mode and also connected to ground.

When a logic 0 is written to the line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the line, otherwise TR1 will remain low impedance.

In telephone applications this switched pull-up source may not be sufficient. Therefore the PCD3343 offers the possibility to select individually 19 of the 20 parallel port pins (not P23), by the following mask options:

Option 1- STANDARD PORT; quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and P-channel booster transistor TR2 (1,5 mA). TR2 is only active during 1 clock cycle (0,28 μs at 3,58 MHz).

Option 2- OPEN DRAIN; quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Fig. 12).

Option 3- PUSH-PULL OUTPUT; drive capability of the output will be 1,5 mA (typ.) at V_{DD} = 3 V in both polarities. To avoid a large current flowing through the output transistors during the input mode, these push-pull pins must only be used as outputs (Fig. 13).

Also, individual mask selection of the RESET state of these port pins can be achieved by appending the following options S and R to options 1, 2 or 3.

Option S-SET; after RESET this pin will be initialized to HIGH.

Option R-RESET; after RESET this pin will be initialized to LOW.

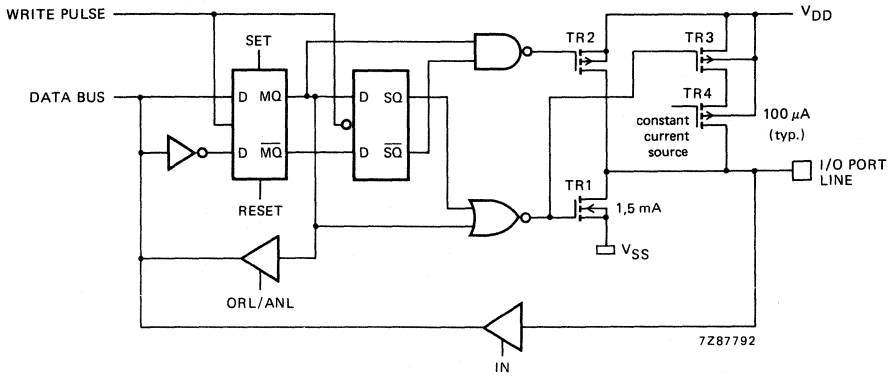


Fig. 11 Standard output with switched pull-up current source.

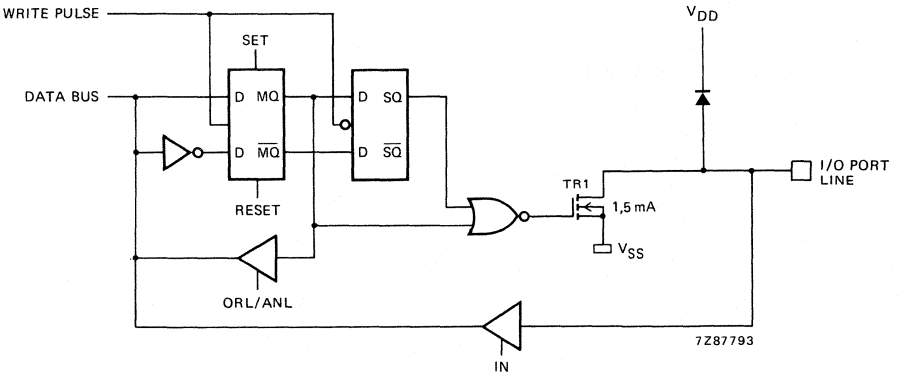


Fig. 12 Open drain output.

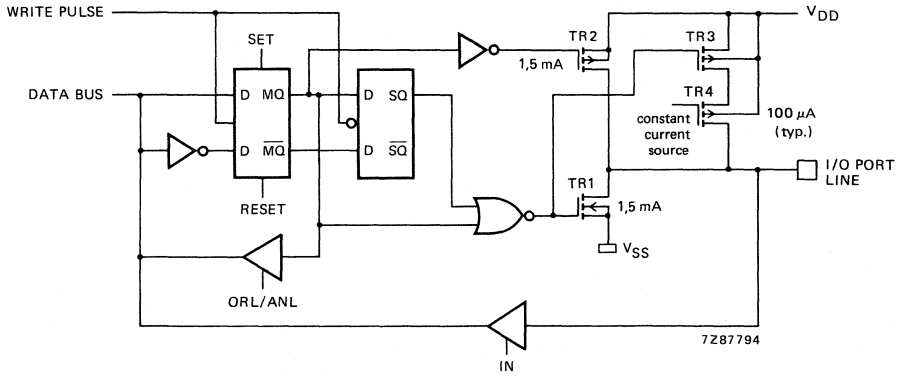


Fig. 13 Push-pull output.

FUNCTIONAL DESCRIPTION (continued)

Serial I/O (SIO)

The PCD3343 has an on-chip serial I/O interface. This SIO interface is a versatile feature in an intelligent telephone set, as shown in application diagram Fig. 32.

In this application the SIO is used to communicate with the different peripherals, such as:

- DTMF generator (PCD3312)
- LCD drivers (PCF8577)
- External RAM (PCD8571)
- Clock calendar (PCB8573)

No extra hardware is required for decoding, addressing and data processing.

Whereas a normal microcontroller must regularly monitor the serial data bus for the presence of data, the serial I/O interface detects, receives and converts the serial data stream into parallel format without interrupting the execution of the current program. An interrupt is sent to the PCD3343 only when a complete byte is received. It then reads the data byte in one instruction. Likewise during transmission the serial I/O interface performs parallel to serial conversion and subsequent serial output of the data. The microcontroller is only interrupted in the execution of its programmed tasks when a complete byte has been transmitted.

The design of the PCD3343 serial I/O system allows any number of devices from PCF8500 family (clips) to be connected via the two-line serial bus. The ability of any devices to communicate, without interrupting the operation of any other devices on the bus, is an outstanding attribute of the system. This is achieved by allocating a specific 7-bit address to each device and providing a system whereby a device reacts only to a message prefixed with its own address or the 'general CALL' address. Address recognition is performed by the interface hardware so that operation of the microcontroller need only be interrupted when a valid address has been received. This saves significant processing time and memory space compared with a conventional microcontroller employing a software serial interface. When the addressing facility is not required, for instance in a system with only two microcontrollers, direct data transfer without addressing can be performed. In multi-master systems, an automatically invoked arbitration procedure prevents two or more devices from continuing simultaneous transmission.

In NORMAL (running) and IDLE mode, the serial I/O logic remains active; its internal system clock will be switched off when there is no activity on the serial bus.

After execution of the STOP instruction, the oscillator of the PCD3343 is switched off. This means that the serial I/O logic will remain in the state it was at the occurance of the STOP instruction. To avoid "bus block" problems and to assure correct start-up of the bus after exit from the STOP mode, the user should disable the serial logic (ESO = 0) prior to the execution of the STOP instruction. This must be carried out only when the PCD3343 has finished a serial data transfer.

Serial I/O interface

Figure 14 shows the serial I/O interface. The clock line of the serial bus has exclusive use of pin 3 (SCLK) while the data line shares pin 2 (serial data) with the I/O line P23 of port 2. When the serial I/O is enabled, P23 is disabled as a parallel port line; (P23 and SCLK only open drain).

The microcontroller and interface communicate via the internal microcontroller bus and the Serial Interrupt Request line. Data and information controlling the operation of the interface are stored in four registers:

- Data shift register (S0)
- Serial I/O interface status word (S1)
- Serial clock control word (S2)
- Address register

Data shift register (S0)

Register S0 converts serial data to parallel format and vice versa. A pending interrupt is generated only after a complete byte has been transmitted, or after a complete data byte, specific address or 'general CALL' address has been received. The most significant bit is transmitted first.

Serial I/O interface status word (S1)

Register S1 provides information concerning the state of the interface and stores information from the microcontroller. Bits 0 to 3 are duplicated: control bits in these positions can only be written by the microcontroller, while interface bits can only be read.

MST and TRX (see Table 1)

These bits determine the operating mode of the serial I/O interface.

Table 1 Operating modes of the serial I/O interface

MST	TRX	operating mode
0	0	slave receiver
1	0	master receiver
0	1	slave transmitter
1	1	master transmitter

BB: Bus Busy.

This is the flag which indicates the status of the bus.

PIN: Pending Interrupt Not

PIN = '0' indicates the presence of a pending interrupt, which will cause a Serial Interrupt Request when the serial interrupt mechanism is enabled.

ESO: Enable Serial output

The ESO flag enables/disables the serial I/O interface: ESO = '1' enables, ESO = '0' disables. ESO can only be written by software.

BC0, BC1 and BC2

Bits BC0, BC1 and BC2 indicate the number of bits received or transmitted in a data stream. These bits can only be written by software.

AL: Arbitration Lost

The arbitration lost flag is set by hardware when the serial I/O interface, as master transmitter, loses a bus arbitration procedure.

AAS: Addressed As Slave

This flag is set by hardware when the interface detects either its own specific address or the 'general CALL' address as the first byte of a transfer and the interface has been programmed to operate in the address recognition mode.

AD0: Address Zero

This flag is set by hardware after detection of the 'general CALL' address when the interface is operating in the address recognition mode.

LRB: Last Received Bit

This contains either the last data bit received or, for a transmitting device in the acknowledgement mode, the acknowledgement signal from the receiving device.

Bits AL, AAS, AD0 and LRB can only be read by software.

FUNCTIONAL DESCRIPTION (continued)

Serial clock control word (S2)

Bits 0 to 4 of the clock control register S2 are used to set the frequency of the serial clock signal. When a 3,58 MHz crystal is used, the frequency of the serial clock can be varied between 92 kHz and 580 Hz (see Table 2). An asymmetrical clock with a HIGH-to-LOW ratio of 3 : 1 can be generated using bit 5. The asymmetrical clock allows a microcontroller more time per clock period for sampling the data line, making the timing of this action less critical. Bit 6 can be used to activate the acknowledge mode of the serial I/O. S2 is a write only register.

Address register

The address register contains the 7-bit address back-up latches and the bit (ALS) used to enable/disable the address recognition mode. The address register can be written using the MOV S0, A and MOV S0, # data instructions, but only when ES0 = '0'.

Serial I/O interrupt logic

An EN SI instruction enables and a DIS SI instruction disables the interrupt logic. When the logic is enabled, a pending interrupt results in a serial I/O interrupt to the processor, causing a CALL to location 5 in the ROM. When disabled, the presence of an interrupt is still indicated by PIN in S1, allowing the interrupt to be serviced. However, vectored interrupt will not occur.

Table 2 SIO clock pulse frequency control when using a 3,58 MHz crystal

hexadecimal S20-S24 code	divisor	f_{SCLK} (kHz) (approximate)
0	not allowed	
1	39	92
2	45	80
3	51	70
4	63	57
5	75	48
6	87	41
7	99	36
8	123	29
9	147	24
A	171	21
B	195	18
C	243	15
D	291	12
E	339	11
F	387	9,2
10	483	7,4
11	579	6,2
12	675	5,3
13	771	4,6
14	963	3,7
15	1155	3,1
16	1347	2,7
17	1539	2,3
18	1923	1,9
19	2307	1,6
1A	2691	1,3
1B	3075	1,2
1C	3843	0,93
1D	4611	0,78
1E	5379	0,67
1F	6147	0,58

FUNCTIONAL DESCRIPTION (continued)

Table 3 Serial I/O addresses for telephony peripherals

type	address 7	6	5	4	3	2	1	0	description
PCF8570A	1	0	1	0	A2	A1	X	R/$\overline{W}$	2 K RAM
PCF8570	1	0	1	0	A2	A1	A0	R/$\overline{W}$	2 K RAM
PCD8571	1	0	1	0	A2	A1	A0	R/$\overline{W}$	1 K RAM
PCD3311	0	1	0	0	1	0	A0	R/$\overline{W}$	DTMF dialler
PCD3312	0	1	0	0	1	0	A0	R/$\overline{W}$	DTMF dialler
PCE2111	0	0	0	0	0	0	1	0	LCD driver *
PCD8573	1	1	0	1	0	A1	A0	R/$\overline{W}$	clock calendar
PCF8574	0	0	1	1	A2	A1	A0	R/$\overline{W}$	8-bit I/O expander
PCF8576	0	1	1	1	0	0	SA0	R/$\overline{W}$	1 : 4 LCD driver
PCF8577	0	1	1	1	0	1	0	R/$\overline{W}$	1 : 2 LCD driver

* LCD driver requires an additional enable line.

DEVELOPMENT SAMPLE DATA

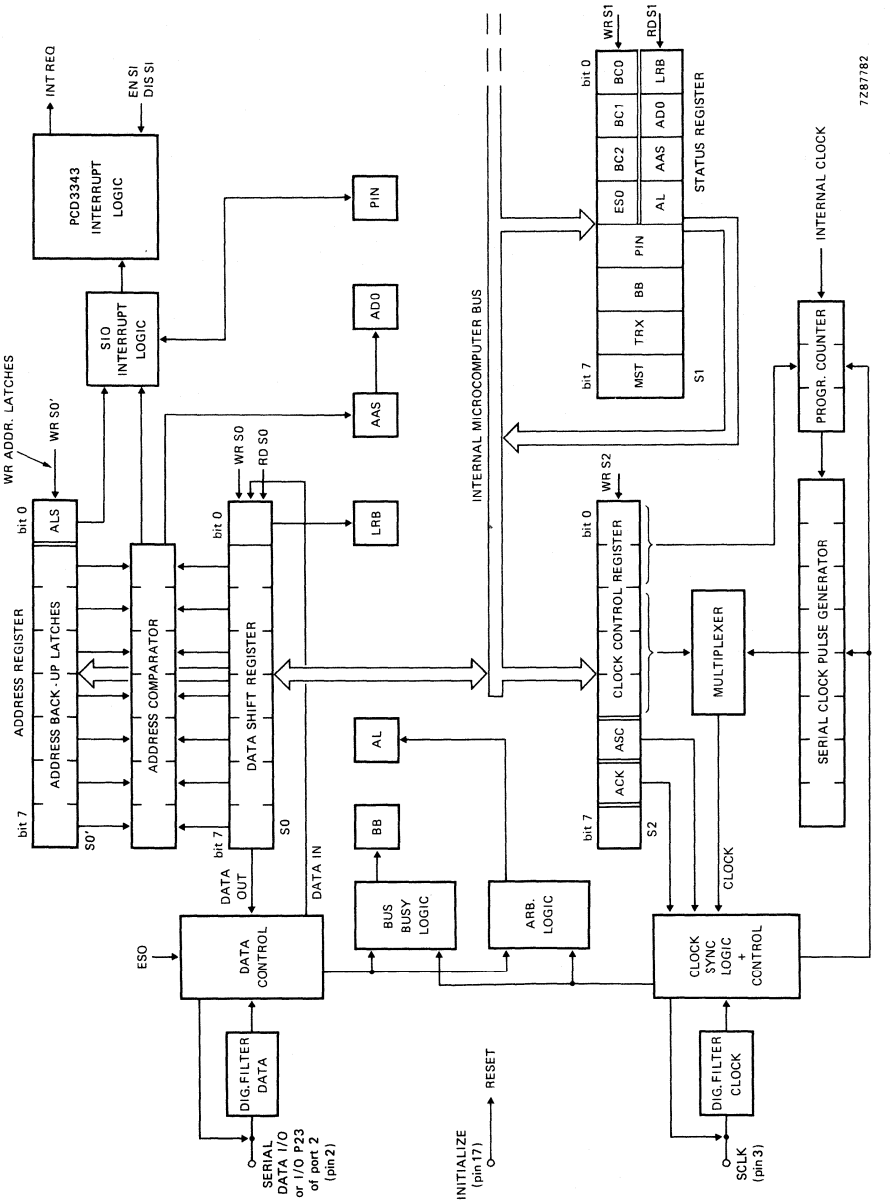


Fig. 14 Serial I/O interface.

FUNCTIONAL DESCRIPTION (continued)

Interrupts (see Fig. 15)

When the external interrupt is enabled, a LOW-to-HIGH transition on the CE/$\overline{T0}$ input initiates an external interrupt subroutine which causes a CALL to program memory location 3 following completion of the current instruction.
The interrupt must remain enabled until the interrupt instruction is completed, otherwise the next instruction of the main program will be executed. Serial I/O interrupt, when enabled, causes a CALL to location 5, and a timer/event counter overflow forces a CALL to location 7 when the timer interrupt is enabled.

When an interrupt subroutine starts, the contents of the program counter and bits 4, 6 and 7 of the PSW have been saved in the program counter stack. Accumulator contents have to be saved by software. Interrupt acknowledgement can be carried out by software via port pins. All interrupt subroutines must reside in memory bank 0.

Since the interrupt system is single level, once an interrupt is detected, all further interrupt requests are latched, but ignored, pending a RETR instruction to re-enable the interrupt input logic. After executing RETR, the program continues in the main part; this is independent of the occurance of a second interrupt during the running of the first routine. If 2 or 3 interrupts occur simultaneously, their priority is:

- (1) external
- (2) serial I/O
- (3) timer/event counter

An external interrupt can be generated by using the timer/counter in the event counter mode. The counter is first preset to (H'FF'), then EN TCNTI instruction is executed. A LOW-to-HIGH transition of the T1 input will then initiate an interrupt subroutine and cause a CALL to location 7.

On execution of a DIS I instruction, the PCD3343 always clears the digital filter/latch and the External Interrupt Flag.

The Timer Flag (TF) is reset only when the JTF or JNTF instruction is executed or after RESET.

The Timer Interrupt Flag is set when timer overflow occurs, only if the timer interrupt is enabled.

The microcontroller will exit the IDLE mode when any one of the following three interrupts is enabled:

- External
- Serial I/O
- Timer/event counter

There is no internal pull-up or pull-down device connected to the external interrupt input (pin 12). If required pin 12 must be externally connected to a resistor ($R \leqslant 100\ k\Omega$). When the external interrupt is not used pin 12 must be connected to V_{SS}.

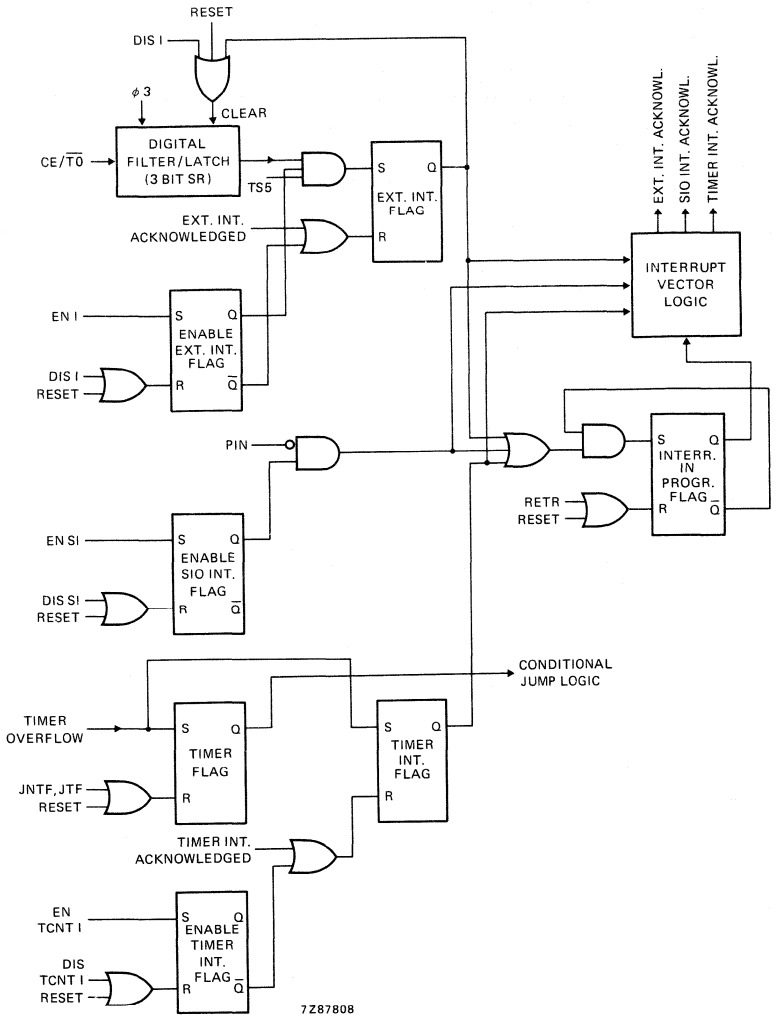


Fig. 15 Interrupt logic.

Notes to figure 15

1. CE/$\overline{T0}$ positive edge is always latched in the digital filter/latch.
2. Correct interrupt timing in ensured when CE/$\overline{T0}$ is LOW for >4 CP followed by a HIGH for >7 CP.
3. When the interrupt in progress flag is set, further interrupts are latched but ignored, until RETR is executed.
4. A DIS I instruction always clears a pending external interrupt.

FUNCTIONAL DESCRIPTION (continued)

Oscillator (see Fig. 16)

The 3,58 MHz oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low-voltage condition is present to prevent discharge of a weak back-up battery.

Provided the supply voltage is within the operating range, the oscillator will be restarted after a STOP instruction by a HIGH level at either the CE/$\overline{T0}$ or RESET pin.

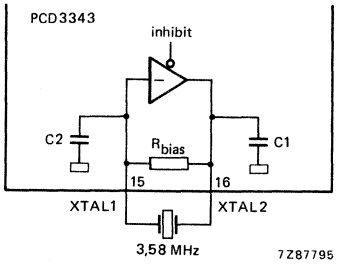


Fig. 16 Oscillator with integrated elements.

The oscillator has the output drive capability for the DTMF generator (PCD3311/3312) via pin 16 (XTAL 2). An external clock can be applied to pin 15 (XTAL 1). A machine cycle consists of 10 time slots, each time slot being 3 oscillator periods.

In telephony applications the 3,58 MHz crystal provides a 8,4 μs machine cycle. The range of the clock frequency is from 100 kHz up to a maximum which is a function of the supply voltage (see Fig. 23).

Timer/event counter (see Fig. 17)

An internal 8-bit up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. Table 4 gives the instructions that control the counter and the prescaler, and the functions performed.

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW-to-HIGH transitions on pin 13 (T1) are counted. The maximum rate at which the counter may be incremented is once every machine cycle (182,6 kHz for a 8,4 μs machine cycle). When the counter overflows, the timer flag is set. The flag can be tested and reset using the JTF (jump if timer flag = 1) or JNTF instruction. Overflow also generates an interrupt to the processor via setting of the Timer Interrpt Flag when the timer/event counter interrupt is enabled.

Table 4 Timer/event counter control

function	timer mode modulo-1, modulo-32*	counter mode
CLEAR	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
PRESET	MOV T,A	MOV T,A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ**	MOV A,T	MOV A,T

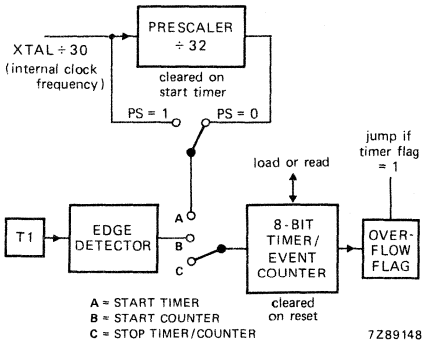


Fig. 17 Timer/event counter.

Program status word (see Fig. 18)

The program status word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.
The PSW bits are:

- Bits 0 to 2 — stack pointer bits (SP_0, SP_1, SP_2)
- Bit 3 — prescaler select (PS); 0 = modulo-32; 1 = modulo-1 (no prescaling)
- Bit 4 — working register bank select (RBS); 0 = register bank 0; 1 = register bank 1
- Bit 5 — not used (1)
- Bit 6 — auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7 — carry (CY); the carry flag indicates that previous operation has resulted in an overflow of the accumulator.

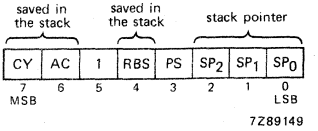


Fig. 18 Program status word.

* With prescaler select, PS = 0, the timer counts modulo-32 machine cycles, with PS = 1 it counts modulo-1 cycles (prescaler not used); prescaler cleared with STRT T, prescaler not readable.

** READ does not disturb the counting process.

FUNCTIONAL DESCRIPTION (continued)

Program status word (continued)

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by a SEL RB instruction, bit 3 by the MOV PSW, A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions and in the event of an interrupt. Bits 7, 6 and 4 are stored in the program counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt and can be used at the end of a normal subroutine. The RET instruction has no restore feature and cannot be used at the end of an interrupt.

Program counter (see Fig. 19)

A 13-bit program counter is used to facilitate 8 K bytes of ROM being addressed. The arrangement of the bits is shown in figure 19. During an interrupt subroutine PC_{11} and PC_{12} are forced to logic 0. All 13 bits are saved in the stack during CALL and interrupt routines.

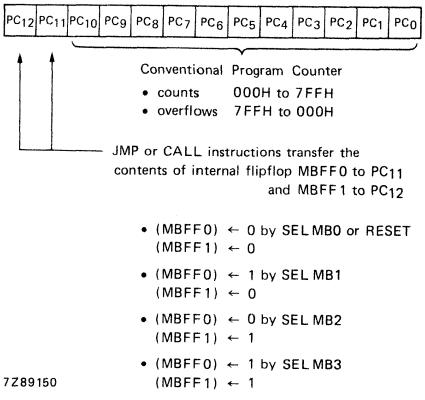


Fig. 19 Program counter.

Central processing unit

The PCD3343 has arithmetic, logical and branching capabilities. The DA A, SWAP A and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the current ROM page.

Conditional branch logic

The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program. Table 5 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

Table 5 Conditional branches

test	jump condition	jump instruction
accumulator	all bits zero	JZ
	any bit non-zero	JNZ
accumulator bit test	1	JB0 to JB7
carry flag	1	JC
	0	JNC
timer overflow flag	1	JTF
	0	JNTF
test input T0	1	JNT0
	0	JT0*
test input T1	1	JT1
	0	JNT1
register	non-zero	DJNZ

Test input T1 (pin 13)

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- JT1 instruction tests for logic 1 level
- JNT1 instruction tests for logic 0 level

When used as an input to the event counter, T1 must be LOW for > 4 CP, followed by a HIGH for > 4 CP. The transition can be recognized with a repetition rate of once per 30 oscillator clock periods (1 machine cycle).

There is no internal pull-up or pull-down resistor connected to the T1 input. If required it must be externally connected to a resistor ($R = \leqslant 100\ k\Omega$). When T1 is not used pin 13 must be connected to V_{DD} or V_{SS}.

Reset (pin 17)

A positive-going signal on the RESET input/output:

- Sets the program counter to zero
- Selects location 0 of memory band 0 and register bank 0
- Sets the stack pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external, timer and serial I/O)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to modulo-32
- Resets the timer flag
- Sets all ports according to reset states
- Sets the serial I/O to slave receiver mode and disables the serial I/O
- Cancels IDLE and STOP mode

After the voltage is applied to RESET an internal delay of 1866 CP is introduced before the microcontroller commences operation.

* Because of the inverted interrupt input CE/$\overline{T0}$ the conditional jump JT0 is also inverted.

FUNCTIONAL DESCRIPTION (continued)

Power-on-reset and low-voltage detection (see Fig. 20)

In telephony applications, correct operation of the PCD3343 during moments of slowly changing supply voltages and low-voltage conditions is essential. This is achieved by the addition of an internal power-on-reset and low-voltage detection circuit.
To allow an external RESET signal being fed into the PCD3343, the reset pin (pin 17) has been configured as an input/output.

While a reset condition exists in the detection circuit, pin 17 is pulled HIGH by TR1 controlled by the reset circuit.
When the reset condition is not present a pull-down current source (TR2) will be activated. TR2 forces pin 17 LOW thus removing the RESET signal from the microcontroller.

Since the level at pin 17 is recognized by the microcontroller, the reset time constant can be stretched by connecting an external capacitor between V_{DD} and pin 17 (see Fig. 22).

The signal at pin 17 can also be used as an output to reset other devices in the system.

The internal reset circuit monitors the PCD3343 supply voltage. If the voltage drops below the switching level (typ. 1,3 V), a reset (HIGH) is applied to pin 17. This reset is removed (pin 17 goes LOW), after a fixed delay (t_d), when the supply voltage rises above the switching level again. The delay ensures a complete reset even when the supply voltage quickly rises above switching level after initial switch-on.

During a low-voltage condition the oscillator is inhibited to prevent complete discharge of a weak battery. The timing of the power-on-reset and low-voltage detection circuit is shown in figure 21.

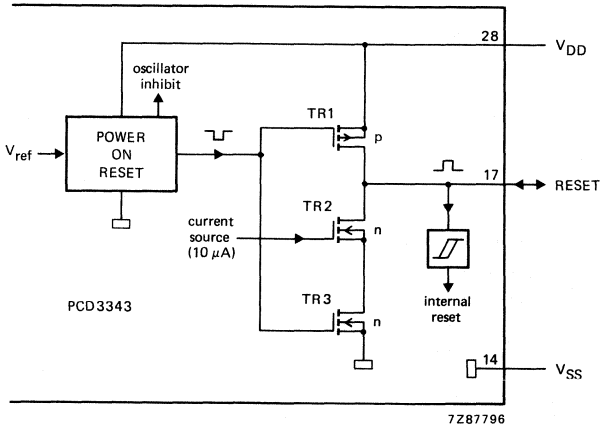
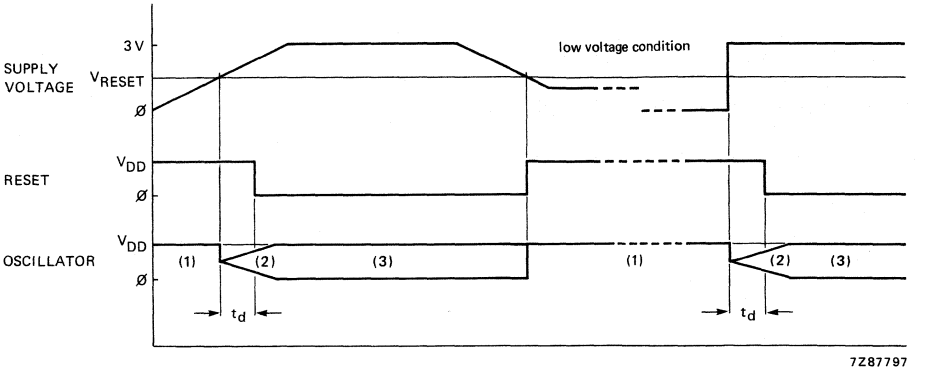


Fig. 20 Power-on-reset configuration.



Where: (1) Oscillator inhibited
(2) Oscillator starting
(3) Oscillator running, but may be stopped with a STOP condition

Fig. 21 Timing of power-on-reset and low-voltage detection.

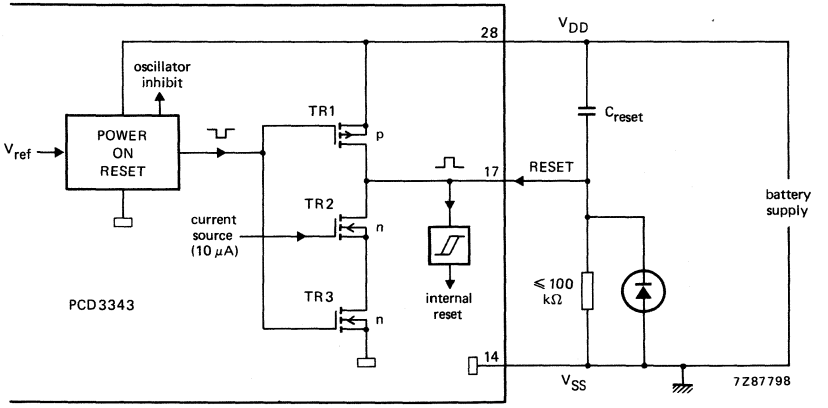


Fig. 22 Stretched power-on-reset with external capacitor.

INSTRUCTION SET

The PCD3343 instruction set consists of over 80 one and two byte instructions and is based on the MAB8048 instruction set. New instructions include those for serial I/O operation and memory bank selection. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 8 gives the instruction set of the PCD3343. Table 7 shows the instruction map and Table 6 details the symbols and definition descriptions that are used.

Table 6 Symbols and definitions used in Table 8

symbol	definition description
A	accumulator
addr	program memory address
Bb	bit designation (b = 0-7)
RBS	register bank select
C	carry bit (bit CY)
CNT	event counter
D	mnemonic for 4-bit digit (nibble)
data	8-bit number or expression
I	interrupt
MB	memory bank
MBFF	memory bank flip-flop
P	mnemonic for 'in-page' operation
PC	program counter
Pp	port designation (p = 0, 1 or 2)
PSW	program status word
RB	register bank
Rr	register designation (r = 0-7)
Sn	serial I/O register
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with

Table 7 PCD3343 instruction map

first hexadecimal character of opcode

second hexadecimal character of opcode

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A,#data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0	1	2		MOV A,Sn 0	1		
1	INC @Rr 0	1	JBO addr	ADDC A,#data	CALL page 0	DIS I	JTF addr	INC A	INC Rr 0	1	2	3	4	5	6	7
2	XCH A,@Rr 0	1	STOP	MOV A,#data	JMP page 1	EN TCNTI	JNTO addr	CLR A	XCH A,Rr 0	1	2	3	4	5	6	7
3	XCHD A,@Rr 0	1	JB1 addr		CALL page 1	DIS TCNTI	JTO addr	CPL A	OUTL Pp,A 0	1	2		MOV Sn,A 0	1	2	
4	ORL A,@Rr 0	1	MOV A,T	ORL A,#data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr 0	1	2	3	4	5	6	7
5	ANL A,@Rr 0	1	JB2 addr	ANL A,#data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr 0	1	2	3	4	5	6	7
6	ADD A,@Rr 0	1	MOV T,A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr 0	1	2	3	4	5	6	7
7	ADDC A,@Rr 0	1	JB3 addr		CALL page 3			RR A	ADDC A,Rr 0	1	2	3	4	5	6	7
8				RET	JMP page 4	EN SI			ORL Pp,#data 0	1	2					
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,#data 0	1	2		MOV Sn,#data 0	1	2	
A	MOV @Rr,A 0	1		MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A 0	1	2	3	4	5	6	7
B	MOV @Rr,#data 0	1	JB5 addr	JMPP @A	CALL page 5	SEL MB3			MOV Rr,#data 0	1	2	3	4	5	6	7
C	DEC @Rr 0	1			JMP page 6	SEL RB0	JZ addr	MOV A,PSW	DEC Rr 0	1	2	3	4	5	6	7
D	XRL A,@Rr 0	1	JB6 addr	XRL A,#data	CALL page 6	SEL RB1		MOV PSW,A	XRL A,Rr 0	1	2	3	4	5	6	7
E	DJNZ @Rr,addr 0	1			JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr, addr 0	1	2	3	4	5	6	7
F	MOV A,@Rr 0	1	JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr 0	1	2	3	4	5	6	7

INSTRUCTION SET (continued)

Table 8 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) −1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1})\leftarrow A_n$ $(A_0)\leftarrow(C)$, $(C)\leftarrow(A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(C)$, $(C)\leftarrow(A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7})\leftrightarrow(A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data		
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3})\leftrightarrow((R0_{0-3}))$ $(A_{0-3})\leftrightarrow((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3)\leftarrow(A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7})\leftarrow(A)$, $(A)\leftarrow((PC))$		
FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1 r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1	
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) – 1 r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) – 1 ((R1))←((R1)) – 1	
BRANCH	JMP addr	● 4 address	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))	
	DJNZ Rr, addr	E* address	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1 r = 0–7 if (Rr) not zero (PC_{0-7})←addr	
	DJNZ @Rr, addr	E0	2/2	decrement RAM data, addressed by Rr by 1 and jump if not zero to addr	((R0))←((R0)) – 1 if ((R0)) not zero (PC_{0-7})←addr	
		E1			((R1))←((R1)) – 1 if ((R1)) not zero (PC_{0-7})←addr	
	JBb addr	▲ 2 address	2/2	jump to addr if Acc. bit b = 1	if b = 1 : (PC_{0-7})←addr b = 0–7	
	JC addr	F6 address	2/2	jump to addr if C = 1	if C = 1 : (PC_{0-7})←addr	
	JNC addr	E6 address	2/2	jump to addr if C = 0	if C = 0 : (PC_{0-7})←addr	
	JZ addr	C6 address	2/2	jump to addr if A = 0	if A = 0 : (PC_{0-7})←addr	
	JNZ addr	96 address	2/2	jump to addr if A is NOT zero	if A≠0 : (PC_{0-7})←addr	
	JT0 addr	36 address	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr	
	JNT0 addr	26 address	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr	
	JT1 addr	56 address	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr	
	JNT1 addr	46 address	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr	
	JTF addr	16 address	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr	4
	JNTF addr	06 address	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr	

TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
	SEL MB2	A5	1/1	select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
	SEL MB3	B5	1/1	select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
	STOP	22	1/1	enter STOP mode		
	IDLE	01	1/1	enter IDLE mode		
SUBROUTINE	CALL addr	▲ 4 address	2/2	jump to subroutine	((SP))←(PC), ($PSW_{4,6,7}$) 6 (SP)←(SP) + 1 (PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	6
	RET	83	1/2	return from subroutine	(SP)←(SP) −1 (PC)←((SP))	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	(SP)←(SP) −1 ($PSW_{4,6,7}$) + (PC)←((SP))	6

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	
	ANL Pp, #data	98 99 9A	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	
	ORL Pp, #data	88 89 8A	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	
SERIAL INPUT/OUTPUT	MOV A, S_n	0C 0D	1/2	move serial I/O register contents to accumulator	(A)←(S0) (A)←(S1)	8
	MOV S_n, A	3C 3D 3E	1/2	move accumulator contents to serial I/O register	(S0)←(A) (S1)←(A) (S2)←(A)	9
	MOV S_n, #data	9C 9D 9E	2/2	move immediate data to serial I/O register	(S0)←data (S1)←data (S2)←data	
	EN SI	85	1/1	enable serial I/O interrupt		
	DIS SI	95	1/1	disable serial I/O interrupt		
	NOP	00	1/1	no operation		

Notes to Table 8

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of JTF and JNTF instructions resets the Timer Flag (TF).

* : 8, 9, A, B, C, D, E, F
● : 0, 2, 4, 6, 8, A, C, E
▲ : 1, 3, 5, 7, 9, B, D, F

5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 1111 P23, P22, P21, P20.
8. (S1) has a different meaning for read and write operation, see serial I/O interface.
9. (S2) is a write only register. Reading S2 will give value FFH.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 28)	V_{DD}		−0,8 to + 8	V
All input voltages	V_I		0,8 to V_{DD} + 0,8	V
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
Total power dissipation (see note)	P_{tot}	max.	500	mW
Power dissipation per output				
except P23, SCLK	P_O	max.	50	mW
P23, SCLK	P_O	max.	180	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C
Operating junction temperature	T_j	max.	125	°C

Note

Thermal resistance (junction to ambient)				
for SOT-117D	$R_{th\ j\text{-}a}$	max.	120	K/W
for SOT-135A	$R_{th\ j\text{-}a}$	max.	60	K/W
for SOT-136A	$R_{th\ j\text{-}a}$	max.	150	K/W

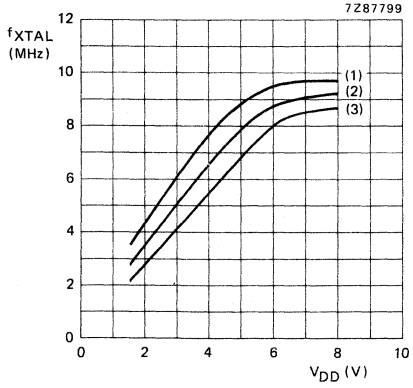
D.C. CHARACTERISTICS

V_{DD} = 2,75 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 50 Ω; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating (see Fig. 23)	V_{DD}	1,8	–	6	V
STOP mode for RAM retention	V_{DD}	1,0	–	6	V
Supply current					
operating					
at V_{DD} = 3 V (see Fig. 24)	I_{DD}	–	600	–	μA
IDLE mode					
at V_{DD} = 3 V (see Fig. 25)	I_{DD}	–	300	–	μA
STOP mode (see Fig. 26 and note 1)					
at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
at V_{DD} = 1,8 V; T_{amb} = 55 °C	I_{DD}	–	–	5	μA
at V_{DD} = 1,8 V; T_{amb} = 70 °C	I_{DD}	–	–	10	μA
RESET I/O					
Switching level	V_{RESET}	–	1,3	–	V
Sink current					
at $V_{DD} > V_{RESET}$	I_{OL}	–	7	–	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	–	V_{DD}	V
Input leakage current					
at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW					
at $V_I = V_{SS}$ or V_{DD}; $\|I_O\| < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW					
at V_{DD} = 3 V; V_O = 0,4 V					
except P23/SDA, SCLK (see Fig. 27)	I_{OL}	0,75	1,5	–	mA
P23/SDA, SCLK (see Fig. 28)	I_{OL}	1,5	–	–	mA
Pull-up output source current HIGH (see Fig. 29)					
at V_{DD} = 3 V; $V_O = 0,9V_{DD}$	$-I_{OH}$	25	–	–	μA
at V_{DD} = 3 V; $V_O = V_{SS}$	$-I_{OH}$	–	–	200	μA
Push-pull output source current HIGH					
at V_{DD} = 3 V; $V_O = V_{DD}$−0,4 V	$-I_{OH}$	0,75	1,5	–	mA

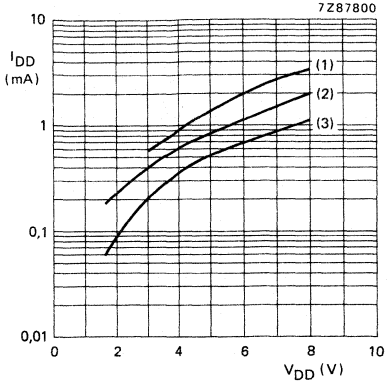
Note 1

Crystal connected between XTAL 1 and XTAL 2; SCL and SDA pulled to V_{DD} via 5,6 kΩ resistor; CE and T1 at V_{SS}.



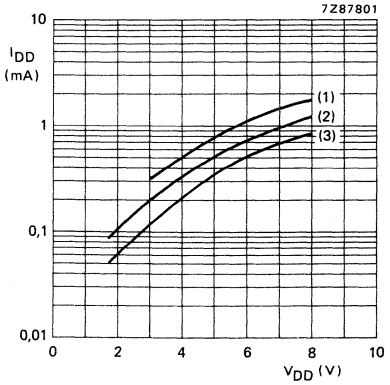
(1) $T_{amb} = -25\ ^{o}C$
(2) $T_{amb} = 25\ ^{o}C$
(3) $T_{amb} = 70\ ^{o}C$

Fig. 23 Maximum clock frequency (f_{XTAL}) as a function of the supply voltage (V_{DD}).



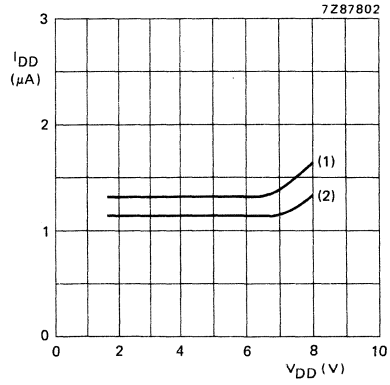
(1) clock frequency = 4 MHz
(2) clock frequency = 2 MHz
(3) clock frequency = 500 kHz

Fig. 24 Typical supply current (I_{DD}) in operating mode as a function of the supply voltage (V_{DD}); $T_{amb} = 25\ ^{o}C$.



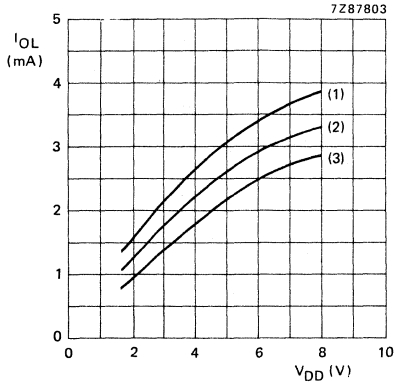
(1) clock frequency = 4 MHz
(2) clock frequency = 2 MHz
(3) clock frequency = 500 kHz

Fig. 25 Typical supply current (I_{DD}) in IDLE mode as a function of the supply voltage (V_{DD}); $T_{amb} = 25\ ^{o}C$.



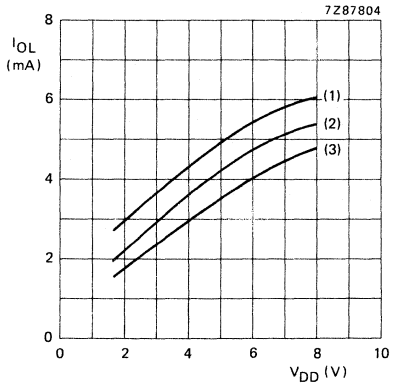
(1) $T_{amb} = 70\ ^{o}C$
(2) $T_{amb} = 25\ ^{o}C$

Fig. 26 Typical supply current (I_{DD}) in STOP mode as a function of the supply voltage (V_{DD}).



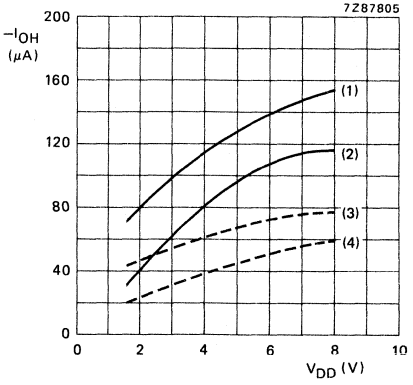
(1) $T_{amb} = -25\ ^{o}C$
(2) $T_{amb} = 25\ ^{o}C$
(3) $T_{amb} = 70\ ^{o}C$

Fig. 27 Output sink current LOW (I_{OL}), except outputs P23/SDA and SCLK, as a function of supply voltage (V_{DD}); V_O = 0,4 V.



(1) $T_{amb} = -25\ ^{o}C$
(2) $T_{amb} = +25\ ^{o}C$
(3) $T_{amb} = +70\ ^{o}C$

Fig. 28 Output current LOW (I_{OL}), outputs P23/SDA and SCLK, as a function of supply voltage (V_{DD}); V_O = 0,4 V.



(1) $T_{amb} = 25\ ^{o}C$; $V_O = V_{SS}$
(2) $T_{amb} = 25\ ^{o}C$; $V_O = 0{,}9V_{DD}$
(3) $T_{amb} = 70\ ^{o}C$; $V_O = V_{SS}$
(4) $T_{amb} = 70\ ^{o}C$; $V_O = 0{,}9V_{DD}$

Fig. 29 Output source current HIGH ($-I_{OH}$) as a function of supply voltage (V_{DD}).

A.C. CHARACTERISTICS

Rise and fall times between 10 and 90% levels; C_L = 50 pF

parameter	symbol	at 70 °C max. value			unit
	V_{DD}	1,8	3,0	6,0	V
Fall time	t_f	200	100	70	ns
Rise time	t_r	200	100	80	ns

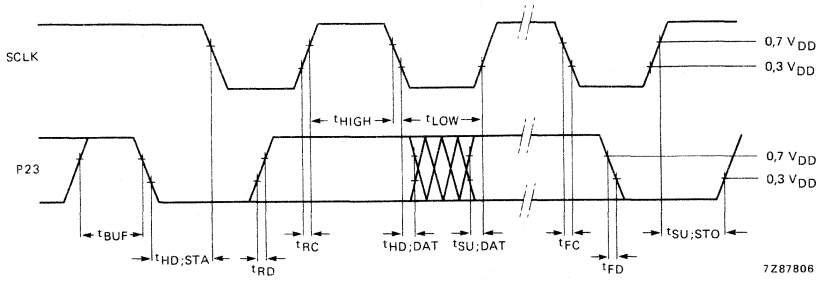


Fig. 30 PCD3343 timing requirements for the P23 and SCLK *input* signals.

Table 9 Input timing shown in figure 30

symbol	timing
t_{BUF}	$\geqslant 14t_{XTAL}$
$t_{HD;STA}$	$\geqslant 14t_{XTAL}$
t_{HIGH}	$\geqslant 17t_{XTAL}$
t_{LOW}	$\geqslant 17t_{XTAL}$
$t_{SY;STO}$	$\geqslant 14t_{XTAL}$
$t_{HD;DAT}$	> 0
$t_{SU;DAT}$	$\geqslant 250$ ns
t_{RD}	$\leqslant 1\ \mu s$
t_{RC}	$\leqslant 1\ \mu s$
t_{FD}	$\leqslant 1\ \mu s$
t_{FC}	$\leqslant 0{,}3\ \mu s$

Notes to Table 9

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 280 ns for f_{XTAL} = 3,58 MHz.
These figures apply to all modes.

A.C. CHARACTERISTICS (continued)

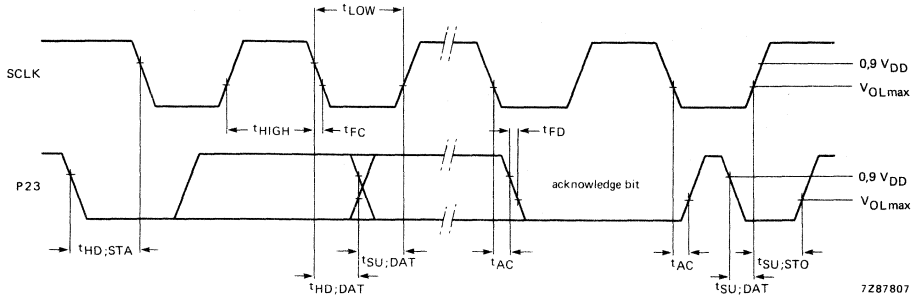


Fig. 31 PCD3343 timing requirements for the P23 and SCLK *output* signals.

Table 10 Output timing shown in figure 31

symbol	timing	
	normal mode (ASC in S2 = 0)	low-speed mode (ASC in S2 = 1)
$t_{HD;STA}$	½ (DF + 9) t_{XTAL}	¾ (DF + 9) t_{XTAL}
t_{HIGH}	½ (DF) t_{XTAL}	¾ (DF) t_{XTAL}
t_{LOW}	½ (DF) t_{XTAL}	¼ (DF) t_{XTAL}
$t_{SU;STO}$	½ (DF − 3) t_{XTAL}	¼ (DF − 3) t_{XTAL}
$t_{HD;DAT}$ (slave transmitter)		
any DF	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{HD;DAT}$ (master transmitter)		
for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	– –
for DF $\leqslant$ 99	– –	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{SU;DAT}$ (master transmitter)		
for DF > 51	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$	– –
for DF > 99	–	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$
for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$	$\geqslant 9t_{XTAL}$
for DF $\leqslant$ 99	–	$\geqslant 9t_{XTAL}$
t_{AC}	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
t_{FD}, t_{FC}	$\leqslant$ 100 ns at C_b = 400 pF	$\leqslant$ 100 ns at C_b = 400 pF

Notes to Table 10

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 280 ns for f_{XTAL} = 3,58 MHz.
DF = divisor (see Table 2 Serial I/O section).
C_b = the maximum bus capacitance for each line.

APPLICATION INFORMATION

A block diagram of an electronic featurephone built around the PCD3343 is shown in figure 32. It comprises the following dedicated telephony IC's:

- TEA1060/1061 transmission circuit for telephony
- PCD3312 DTMF generator with Serial I/O
- PCE2111 or PCF8577 2 LCD drivers in LCD module MB7020160
- PCD8571 1 K RAM's with Serial I/O; the number of RAM's depends on the required amount of stored telephone numbers
- PCD3360/3361 programmable multi-tone ringer

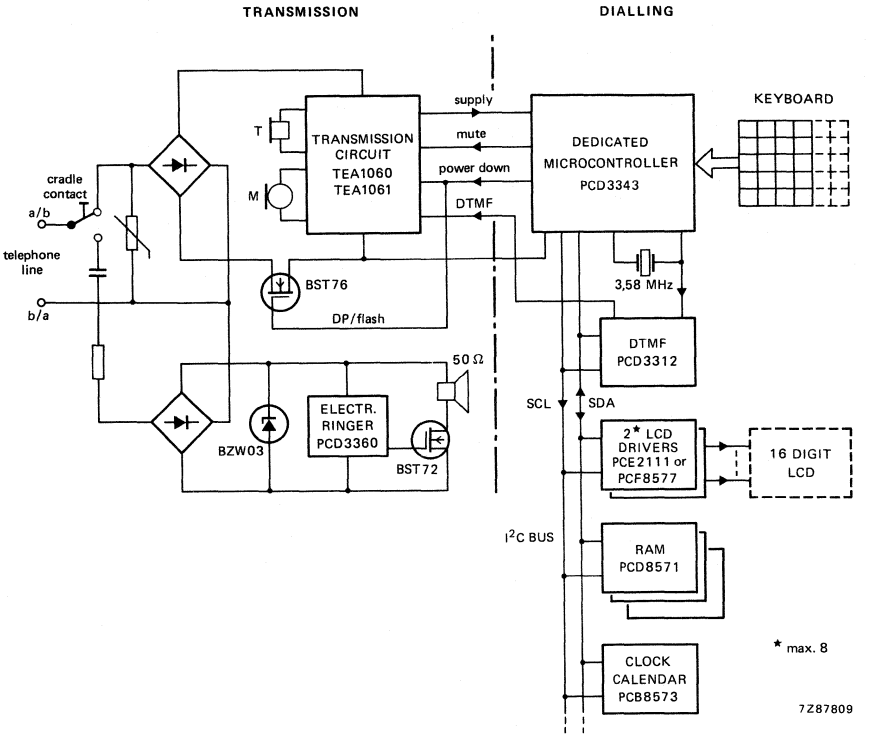


Fig. 32 Block diagram of electronic featurephone with common line interface.

A detailed application diagram of the PCD3343 with PCD3312 (DTMF), two PCD8571 (RAM) and two PCE2111 (LCD display drivers) is shown in figure 33.

Row 5 of the keyboard contains the following special keys:

- P program and autodial
- FL flash or register recall
- R redial or extended redial
- AP access pause

Row 6 contains the different diode options.

Columns 5 and 6 contain the button keys M0 to M9; single name keys for repertory telephone numbers.

APPLICATION INFORMATION (continued)

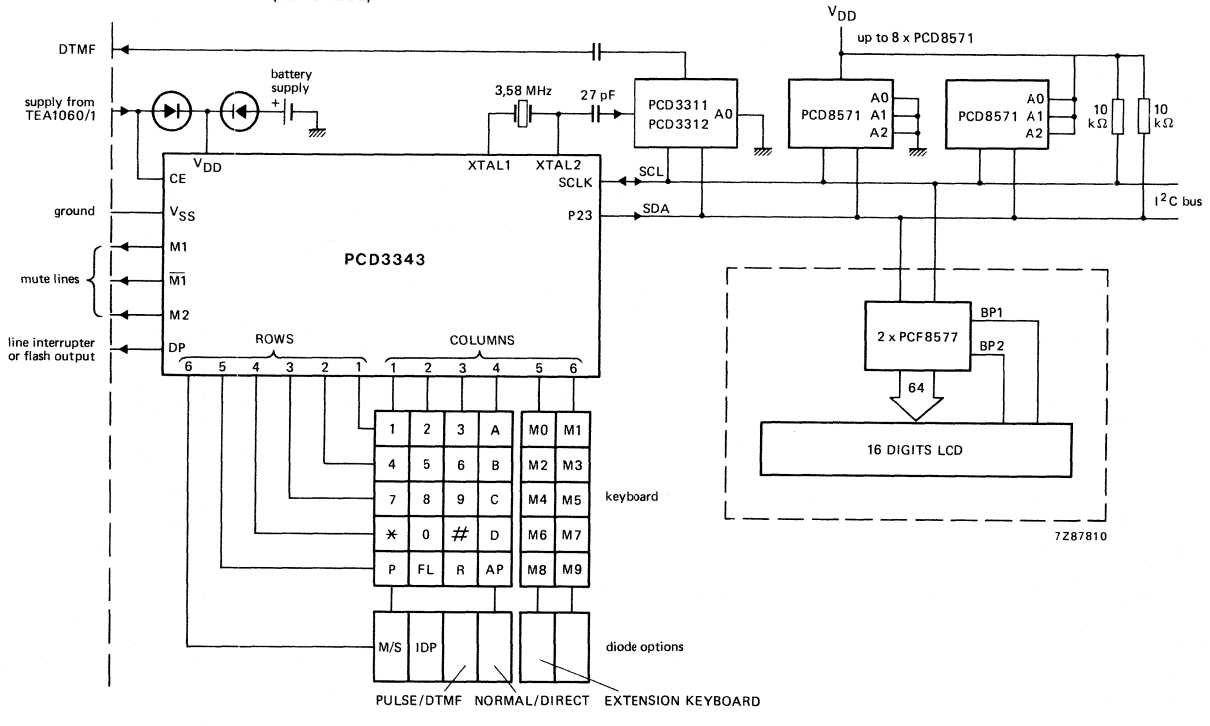


Fig. 33 Application diagram of PCD3343 for electronic featurephone with associated keyboard.

Additional information is available on request for the following:

- Serial I/O
- I^2C bus specification
- Interrupt logic
- Instruction set descriptions
- Software routines for an intelligent telephone set

PROGRAMMABLE MULTI-TONE TELEPHONE RINGER

GENERAL DESCRIPTION

The PCD3360/61 are CMOS integrated circuits, designed to replace the electro-mechanical bell in telephone sets. They meet most postal requirements, particularly with tone sequence possibilities and input frequency selectivity. Output signals for a loudspeaker or for a piezo-electric (PXE) transducer are provided. In the former application, no audio transformer is required since the loudspeaker is driven in class D.

Features

- Output signals for electro-dynamic transducer (loudspeaker) or for piezo-electric transducer (PXE)
- 7 basic frequencies (tones) and a pause
- 4 selectable tone sequences
- 4 selectable repetition rates
- 3 selectable impedance settings
- 3-step automatic swell } loudspeaker only
- Delta-modulated output signal that approximates a sinewave } loudspeaker only
- Input frequency discriminator with selectable upper and lower frequency limits
- Output for optical signal

Note

Tone sequences (up to 16 tones long), impedance settings and automatic swell levels are mask programmable for customized versions.

QUICK REFERENCE DATA

Available frequencies (tones)		533/600/667/800/ 1000/1067 and 1333	Hz
Number of intervals per tone sequence		15 or 16	
Lower limits of frequency discriminator		13,33 or 20	Hz
Upper limits of frequency discriminator		30 or 60	Hz
Impedance settings (with 50 Ω loudspeaker)	approx.	7 or 10,5 or 17,5	kΩ
Switch-on delay at 25 Hz	max.	60	ms

PACKAGE OUTLINES

PCD3360P: 16-lead DIL; plastic (SOT-38).
PCD3361P: 8-lead DIL; plastic (SOT-97EE).
PCD3360T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).
PCD3361T: 8-lead mini-pack; plastic (SO-8L; SOT-176).

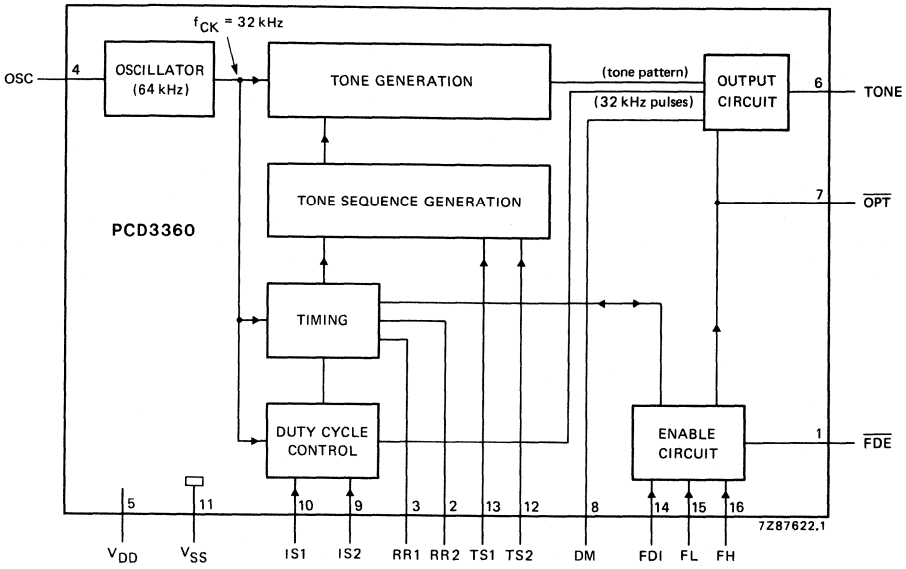


Fig. 1 Block diagram.

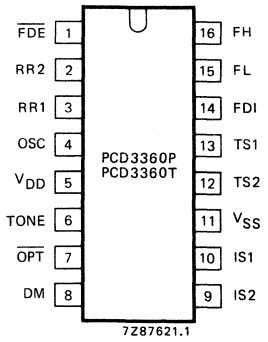


Fig. 2 Pinning diagram for PCD3360P and PCD3360T.

PINNING

1	$\overline{PDE}$	frequency descriminator enable
2	RR2	repetition rate selection
3	RR1	
4	OSC	oscillator
5	V_{DD}	positive supply
6	TONE	tone output
7	$\overline{OPT}$	optical signal output
8	DM	drive mode selection
9	IS2	impedance setting and automatic swell
10	IS1	
11	V_{SS}	negative supply
12	TS2	tone sequence selection
13	TS1	
14	FDI	frequency discriminator input
15	FL	lower frequency limit selection
16	FH	upper frequency limit selection

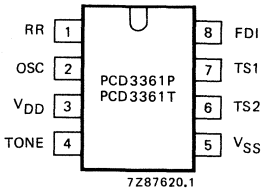


Fig. 3 Pinning diagram for PCD3361P and PCD3361T.

PINNING

1	RR	repetition rate selection
2	OSC	oscillator
3	V_{DD}	positive supply
4	TONE	tone output
5	V_{SS}	negative supply
6	TS2	tone sequence selection
7	TS1	
8	FDI	frequency discriminator input

Note

PCD3360 pins not available in the PCD3361 are at V_{SS}.

FUNCTIONAL DESCRIPTION (see Fig. 1)

Supply pins (V_{DD} and V_{SS})

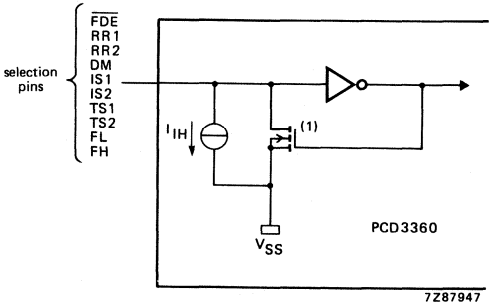
If the supply voltage (V_{DD}) drops below the standby voltage (V_{SB}), the oscillator and most other functions are switched off and the supply current is reduced to the standby current (I_{SB}). The automatic swell register retains its information until V_{DD} drops further to a value V_{AS} at which reset occurs.

Oscillator (OSC)

The 64 kHz oscillator is operated via an external resistor and capacitor connected to pin OSC. The oscillator signal is divided by two to provide the 32 kHz internal system clock.

Selection pins ($\overline{FDE}$, RR2, RR1, DM, IS2, IS1, TS2, TS1, FL and FH)

These pins are pulled down internally by a pull-down current I_{IH} when they are connected to V_{DD}, and by a pull-down resistance R_{IL} when they are connected to V_{SS} (see Fig. 4). Thus when the pins are open-circuit they are defined LOW. Therefore only a single-contact switch is required to connect the pins to V_{DD}; yet the supply current is only marginally increased as I_{IH} is very small.



(1) Transistor resistance = R_{IL} when switched on.

Fig. 4 Input circuit of selection pins.

Frequency discriminator circuit (pins $\overline{FDE}$ and FDI)

The frequency discriminator circuit prevents the ringer being activated by dial pulses, speech or other unqualified signals.

The circuit is enabled or disabled by input $\overline{FDE}$.

When $\overline{FDE}$ is HIGH, FDI acts as a logic enable input.
The circuit will produce tone sequences provided FDI is HIGH and V_{DD} exceeds V_{SB}.
When $\overline{FDE}$ is LOW, FDI acts as the frequency discriminator input.
The circuit will produce tone sequences provided V_{DD} exceeds V_{SB} and the signal at FDI fulfils the conditions set by FL and FH.

When the frequency discriminator is enabled ($V_{DD} > V_{SB}$ and $\overline{FDE}$ = LOW) the circuit will start to produce tone sequences after two rising or two falling edges have occurred at FDI. The time between these edges must be within the limits set by FL and FH.

The circuit will continue to produce tone sequences provided the time between subsequent falling edges or between subsequent rising edges remains within the limits set by FL and FH, otherwise it will stop. Because two edges are required for detection, either positive or negative, the switch-on delay will vary between 1 and 1,5 cycles of the incoming ringing frequency.

FDI has a Schmitt-trigger action; the levels are set by an external resistor R2 (see Fig. 9) and an internal sink current that is switched from 20 μA (typ.) for FDI = LOW to $< 0{,}1$ μA for FDI = HIGH. Excess current entering FDI via R2 is absorbed by internal diodes clamped to V_{DD} and V_{SS}.

Selection of frequency discriminator limits (FL and FH)

With the frequency discriminator enabled ($V_{DD} > V_{SB}$ and $\overline{FDE}$ = LOW) the lower and upper limits of the input frequency are set by inputs FL and FH as shown by Table 1 and Table 2 respectively.

Table 1 Selection of lower frequency discriminator limits (f_{osc} = 64 kHz)

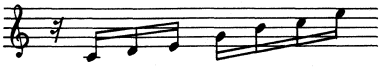
FL input state	lower discriminator limit (Hz)
LOW	20
HIGH	13,33

Table 2 Selection of upper frequency discriminator limits (f_{osc} = 64 kHz)

FH input state	upper discriminator limit (Hz)
LOW	60
HIGH	30

Selection of tone sequences (TS1 and TS2)

A tone sequence is composed of 15 or 16 equal time intervals. Each time interval may be filled with one of seven available tones or with a pause; these are shown together with their corresponding internal ROM tone code in Fig. 5.



tone key	–	c	d	e	g	b	c	e
frequency (Hz)	0	533	600	667	800	1000	1067	1333
frequency ratio		8	9	10	12	15	16	20
tone code	0	1	2	3	4	5	6	7

7Z87948

Fig. 5 Available tones and their corresponding internal ROM tone code.

FUNCTIONAL DESCRIPTION (continued)

Four tone sequences are programmed in the internal ROM (see Fig. 6). Inputs TS1 and TS2 determine which tone sequence is selected and output at pin TONE. The sequences are mask programmable with any length up to 16 time intervals.

The tone sequences are repeated continuously provided the enable conditions at inputs $\overline{FDE}$ and FDI are valid and $V_{DD} > V_{SB}$; the first sequence always starts with the first tone shown in Fig. 6.

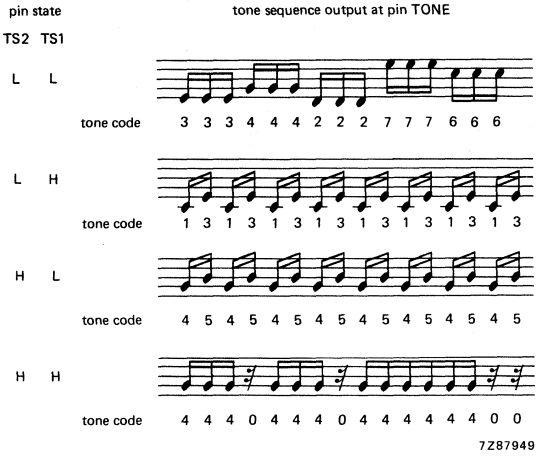


Fig. 6 Tone sequences mask-programmed in the PCD3360/61.

Selection of repetition rates (RR1 and RR2)

The duration of a time interval within a tone sequence is determined by the state of inputs RR1 and RR2 as shown in Table 3. The resultant variation of repetition rate acts as a distinguishing feature between adjacent telephones.

Table 3 Duration of time intervals (f_{osc} = 64 kHz)

input state		time interval
RR1	RR2	ms
L	L	15
L	H	30
H	L	45
H	H	60

The repetition rate variation can be extended by mask programming (for customer defined versions) the same tone combination for all 4 tone sequences, but with a different number of time intervals per tone. Thus the repetition rate can be selected from 16 values by inputs RR1, RR2, TS1 and TS2.

Drive mode selection (DM)

The output signal at pin TONE can be selected for application with electro-dynamic or piezo-electric transducers. An example of both signals, for a tone frequency of 667 Hz, is shown in Fig. 7.

Loudspeaker mode

In the loudspeaker mode (DM = LOW), pin TONE outputs a delta-modulated signal that approximates a sinewave sampled at a rate of 32 kHz. The output pulse duration is determined by pins IS1 and IS2. The resultant acoustic spectrum is aurally more acceptable and has greater penetration than a square wave spectrum because more power is concentrated at the fundamental frequency.

PXE mode

In the PXE mode (DM = HIGH), pin TONE outputs a square wave. In this mode the ringer impedance and sound pressure level are determined by the characteristics (e.g. the size) of the PXE transducer; inputs IS1 and IS2 are inactive.

Setting of impedance, sound pressure level and automatic swell (IS1 and IS2)

With DM = LOW (loudspeaker mode), inputs IS1 and IS2 determine the pulse duration of the output signal and thereby the d.c. resistance R_{xy} (seen at points x and y in Fig. 9) and also the Sound Pressure Level (SPL). The selection of 3 impedance settings and automatic swell is shown in Table 4.

Table 4 Setting of pulse duration and automatic swell (DM = LOW)

input state		function	ringing burst number (N)	pulse duration (μs)		R_{xy} (kΩ)	Z_I (kΩ)	SPL (dBr)
IS1	IS2			fund.	harm.			
L	L	automatic swell	1	1,8	–	40	tbf	tbf
			2	2,6	–	20	17,5	–4
			> 2	3,9	1,6	5	7	0
L	H	constant level	–	2,6	–	20	17,5	–4
H	L		–	3,6	–	10	10,5	tbf
H	H		–	5,0	–	5	7	0

Where:

1. Typical pulse duration values of the fundamental and harmonic frequencies are for f_{osc} = 64 kHz and f_{CK} = 32 kHz.
2. SPL is the relative Sound Pressure Level, and 0 dBr is defined as the SPL for IS1 = IS2 = HIGH.
3. Values of the d.c. resistance R_{xy}, bell impedance (Z_I) and SPL are valid for a value of input voltage V_I = 40 V_{rms} in Fig. 9.

FUNCTIONAL DESCRIPTION (continued)

Setting of impedance, sound pressure level and automatic swell

When pins IS1 and IS2 are both LOW, the circuit operates in the automatic swell mode. The SPL then increases in three steps so that the maximum level is reached for the third ringing burst.
Each time V_{DD} drops below V_{AS} the automatic swell register is reset and the next ringing burst is considered as N = 1 (see Table 4).
A buffer capacitor C3 (see Fig. 9) must hold $V_{DD} > V_{AS}$ during the time between two consecutive ringing bursts of a series.

For each of the other three combinations of pins IS1 and IS2 the pulse duration has a constant value. Thus the ringer can be designed so that the impedance represented at the telephone line will comply with postal requirements that vary in relation to parallel or series connections of more than one ringer.

To satisfy some applications, a harmonic signal is added to the fundamental frequency in the last step of the automatic swell mode. The pulses representing this harmonic signal are interleaved with the pulses of the fundamental signal (see Fig. 8). The difference in pulse duration shown in Table 4, is chosen so that the harmonic level is 10 dB below the fundamental level.
The harmonic frequency range is from 2 kHz to 3,2 kHz. The individual harmonic frequencies for the seven tone codes and the relative fundamental frequencies are shown in Table 5.

Table 5 Harmonic frequency in relation to tone code and fundamental frequency

tone code	frequency (Hz)	
	fundamental	harmonic
1	533	3200
2	600	2400
3	667	2667
4	800	3200
5	1000	2000
6	1067	2133
7	1333	2667

Using a single mask it is possible to program the following:–

- Addition of harmonics in all the other input states of IS1 and IS2
- All pulse duration values
- Other even harmonic frequencies.

Optical output ($\overline{OPT}$)

The $\overline{OPT}$ output is designed to drive an optical signal transducer or lamp. It is LOW when the ringer circuit is enabled and HIGH when the ringer circuit is disabled. This output can also be used to switch the transmitter ON and OFF in the base of a cordless telephone set.

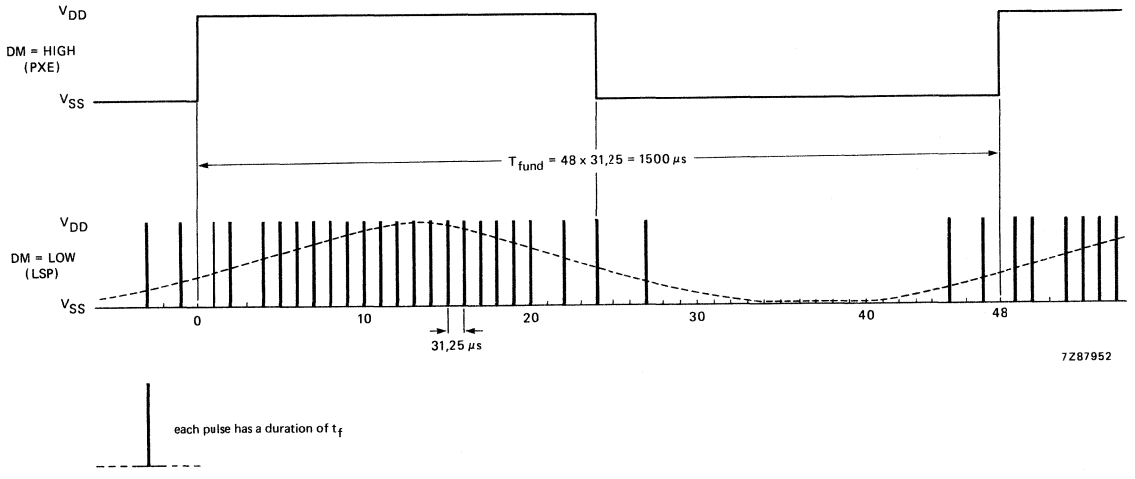


Fig. 7 Fundamental signal (667 Hz) at pin TONE
(for f_{osc} = 64 kHz, to provide f_{CK} = 32 kHz).

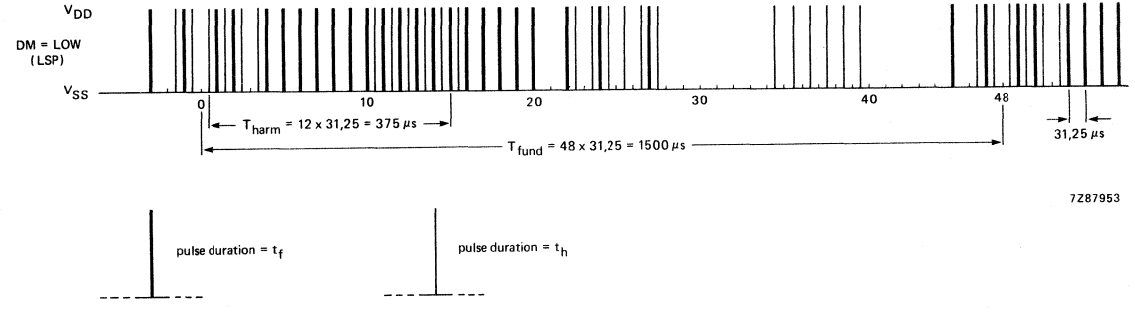


Fig. 8 Fundamental signal (667 Hz) + harmonic signal (2667 Hz) at pin TONE
(for f_{osc} = 64 kHz, to provide f_{CK} = 32 kHz).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to + 9	V
Supply current	I_{DD}	max.	50	mA
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8	V
Total power dissipation	P_{tot}	max.	300	mW
Total dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

D.C. CHARACTERISTICS

V_{DD} = 6 V; V_{SS} = 0; f_{osc} = 64 kHz; T_{amb} = −25 to + 70 °C; valid enable conditions at FDI and $\overline{FDE}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	V_{SB}+0,1	–	8,0	V
Standby supply voltage (note 1)	V_{SB}	tbf	4,8	5,7	V
Supply voltage for automatic swell reset (note 2)	V_{AS}	–	0,5V_{SB}	–	V
Operating supply current	I_{DD}	–	100	120	μA
Standby supply current at $V_{DD} < V_{SB}$ (note 3)	I_{SB}	–	4	8	μA
Inputs					
Input voltage LOW (any pin)	V_{IL}	0	–	0,3V_{DD}	V
Input voltage HIGH (any pin)	V_{IH}	0,7V_{DD}	–	V_{DD}	V
Pull-down circuits of inputs					
$\overline{FDE}$, RR1, RR2, DM, IS1, IS2, TS1, TS2, FL, FH					
pull-down resistance with input at V_{SS}	R_{IL}	–	20	–	kΩ
pull-down current with input at V_{DD}	I_{IH}	–	0,1	–	μA
Pull-down circuit of FDI					
pull-down current with V_{FDI} = 0,3V_{DD}	I_{SL}	tbf	20	tbf	μA
pull-down current with V_{FDI} = 0,7V_{DD}	I_{SH}	–	0,1	–	μA
pull-down current with $V_{DD} < V_{SB}$	I_{SX}	–	0,1	–	μA
Current into input FDI (note 4)	± I_{IS}	–	–	0,2	mA
Outputs					
TONE, $\overline{OPT}$					
Output sink current at V_{OL} = 0,5 V	I_{OL}	1	2	–	mA
Output source current at V_{OH} = V_{DD}−0,5 V	$-I_{OH}$	1	2	–	mA

DEVELOPMENT SAMPLE DATA

Notes see next page.

A.C. CHARACTERISTICS

V_{DD} = 6 V; V_{SS} = 0; f_{osc} = 64 kHz; T_{amb} = −25 to + 70 °C; valid enable conditions at FDI and $\overline{FDE}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Switch-on delay (with $\overline{FDE}$ = LOW and ringing frequency within limits set by FL and FH)	$t_{d(on)}$	1	–	1,5	note 5
Switch-off delay (with $\overline{FDE}$ = LOW)					
at FL = LOW	$t_{d(off)}$	–	–	75	ms
at FL = HIGH	$t_{d(off)}$	–	–	112,5	ms
Oscillator frequency at R_{osc} = 365 kΩ; C_{osc} = 56 pF (note 6)	f_{osc}	tbf	64	tbf	kHz
Frequency variation at V_{DD} = 5,7 to 8,0 V	Δf_{osc}	–	–	1	%

Notes to the characteristics

1. For $V_{DD} < V_{SB}$ the circuit is in standby.
2. At $V_{DD} = V_{AS}$ the automatic swell register is reset.
3. The standby supply current is measured with all inputs and outputs open-circuit with the exception of OSC.
4. The current I_{IS} is clamped to V_{DD} and to V_{SS} by two internal diodes. Correct operation is ensured with $V_{FDI} > V_{DD}$ or $V_{FDI} < V_{SS}$, provided the maximum value of I_{IS} is not exceeded. (The input FDI has an extended HIGH and LOW input voltage range.)
5. The switch-on delay is measured in cycles of incoming ringing frequency.
6. Lead lengths of R_{osc} and C_{osc} to be kept to a minimum.

APPLICATION INFORMATION

Application of the PCD3360 in a telephone ringer circuit together with a loudspeaker is shown in Fig. 9.

The threshold levels V_H and V_L of the frequency discriminator circuit are determined by:

- The logic threshold of input FDI ($0{,}5V_{DD}$ typ. 3,4 V for V_{DD} = 6,8 V)
- The pull-down current of input FDI (20 μA typ. for FDI $<$ 3,4 V)
- The value of R2 (680 kΩ in Fig. 9)

For a positive slope, the voltage at R2 must exceed the value V_H before FDI will become HIGH; V_H is the sum of the input threshold and the voltage drop across R2 thus:

$$V_H = 3{,}4 + (680 \times 10^3) \times (20 \times 10^{-6}) = 17 \text{ V}.$$

For a negative slope, the voltage at R2 must decrease below the value V_L before FDI will become LOW. Because the current into FDI is negligible with FDI = HIGH the voltage drop across R2 can be discounted, thus V_L = 3,4 V.

The minimum operating voltage across C3 is 17,7 V which is determined by:

- The minimum operating voltage of the PCD3360 (5,7 V)
- The supply current of the PCD3360 (120 μA max.)
- The value of R2 (100 kΩ in Fig. 9)

The total switch-on delay equals approximately the time required to charge the supply capacitor C3 to the minimum operating value, plus the specified switch-on delay of the PCD3360.

The high operating voltage combined with the class D output stage ensures optimal energy conversion and thereby a high sound level. The design can easily be optimized for parallel or series connection of more than one ringer. The diode bridge, zener diode (D1) and resistor R1 protect the ringer against transients up to 5 kV. During these surges the voltage on the 68 V zener diode (BZW03) can rise to 100 V; the DMOS transistor BST72 (TR1) has a maximum drain-source voltage of 100 V. Up to 220 V, 50 Hz can be applied to the a/b terminals without damaging the ringer.
The choke (L1) in series with the 50 Ω loudspeaker increases the sound pressure level by approximately 3 dB by suppression of the 32 kHz carrier frequency and its sidebands.
The flyback diode BAX18A (D2) is a fast type with low forward voltage to obtain high efficiency.

Application of the PCD3360 together with a PXE transducer is shown in Fig. 10. The only significant difference between Fig. 9 and Fig. 10 is the output stage. Two BST72 transistors provide an output voltage swing almost equal to the voltage at C3. Pins IS1 and IS2 are inoperative because DM = HIGH. Volume control is possible using resistor R_V.

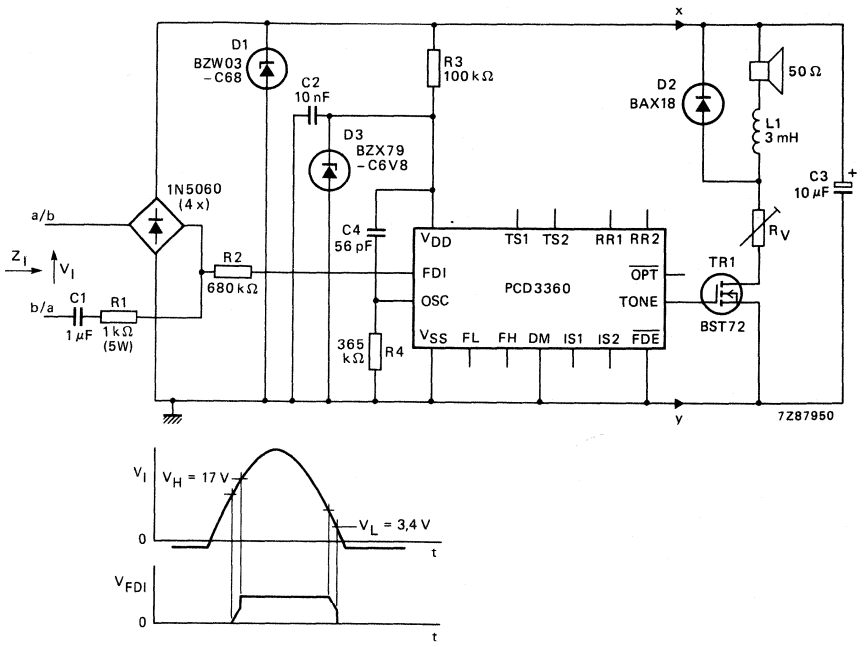


Fig. 9 Transformerless electronic ringer with PCD3360 and a loudspeaker.

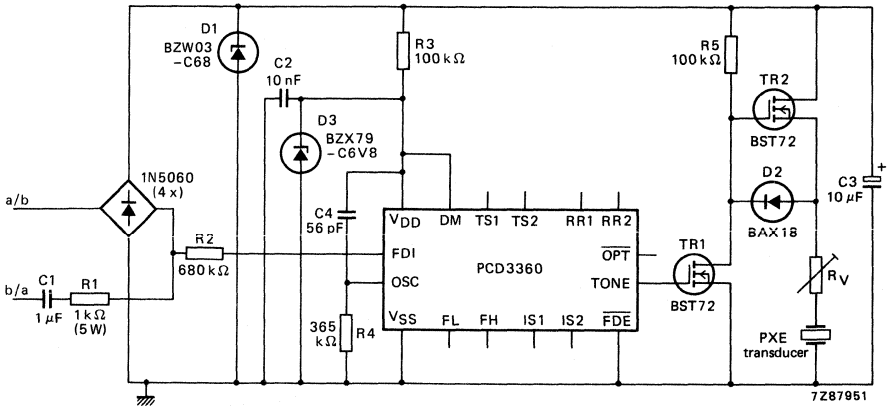


Fig. 10 PCD3360 ringer with PXE transducer.

256 × 4-BIT STATIC RAM

GENERAL DESCRIPTION

The PCD5101 is a very low-power 1024-bit static CMOS random access memory, organized as 256 words by 4 bits. It is suitable for low power and high speed applications where battery standby power is required to ensure non-volatility of data. All inputs and outputs are fully TTL compatible and pinning is compatible with 2101-type NMOS static RAMs and 5101-type CMOS static RAMs.

There are two chip enable inputs, $\overline{CE1}$ and CE2, selection being made when $\overline{CE1}$ is LOW and CE2 is HIGH. The memory has an output disable function, OD, which allows the inputs/outputs to be used separately, or to be tied together for use in common data I/O systems.

Features

- Operating supply voltage range 2,5 to 5,5 V
- Low data retention voltage min. 1 V
- Low power consumption in both operating and standby modes
- Access time 150 ns at V_{DD} = 5 V; 400 ns at V_{DD} = 3 V
- Three-state outputs
- All inputs and outputs directly TTL compatible
- Choice of two package types

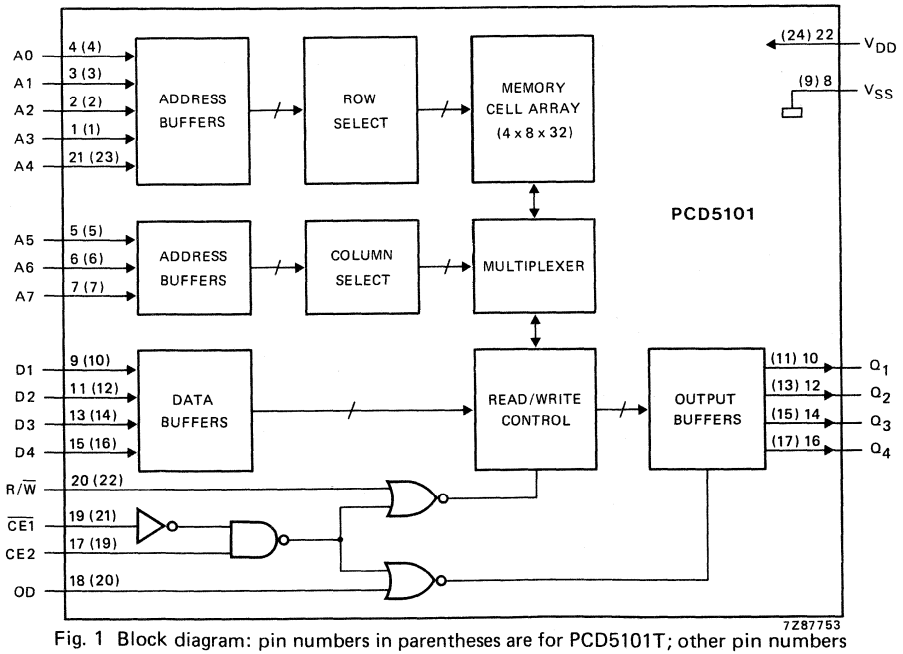


Fig. 1 Block diagram: pin numbers in parentheses are for PCD5101T; other pin numbers are applicable to PCD5101P.

PACKAGE OUTLINES

PCD5101P: 22-lead DIL; plastic (SOT-116).
PCD5101T: 24-lead mini-pack; plastic (SO-24; SOT-137A).

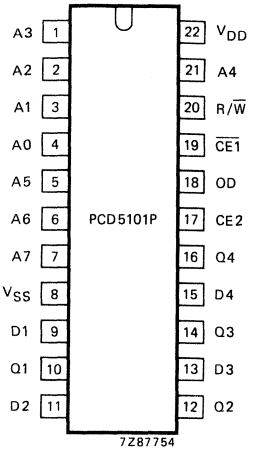


Fig. 2 Pinning diagram for PCD5101P.

PINNING

D1, D2, D3, D4	data inputs
A0, A1, A2, A3, A4, A5, A6, A7	address inputs
R/$\overline{W}$	read/write input
$\overline{CE1}$, CE2	chip enable inputs
OD	output disable
Q1, Q2, Q3, Q4	data outputs
V_{DD}	positive supply
V_{SS}	negative supply
n.c.	not connected

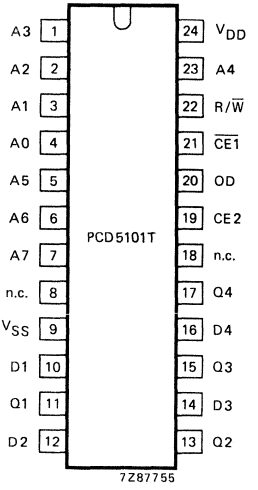


Fig. 3 Pinning diagram for PCD5101T.

OPERATING MODES

Table 1 Mode selection

$\overline{CE1}$	CE2	R/$\overline{W}$	OD	mode of operation	output state
H	X	X	X	standby	high impedance
X	L	X	X	standby	high impedance
L	H	L	H	write	high impedance
L	H	L	L	write	equal to input data
L	H	H	L	read	data valid
L	H	H	H	read	high impedance

Separate input/output: write cycle OD = X; read cycle OD = L.

Common input/output: write cycle OD = H; read cycle OD = L.

H = HIGH voltage level
L = LOW voltage level
X = don't care

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to 8,0 V
Input voltage range (any pin)	V_I	V_{SS} − 0,3 to V_{DD} +0,3 V
Operating temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +125 °C

D.C. CHARACTERISTICS (V_{DD} = 5 V)

V_{DD} = 5 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	4,5	5,0	5,5	V
Operating supply current					
at V_I = V_{DD} or V_{SS}; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 or 2,0 V; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 or 2,0 V; f = 5 MHz; outputs open	I_{DD}	–	12	20	mA
Standby supply current at CE2 = V_{SS}	I_{SB}	–	0,02	5,0	μA
Input leakage current at V_I = V_{SS} to V_{DD}	$\|I_{IL}\|$	–	–	0,1	μA
Input voltage LOW	V_{IL}	−0,3	–	+0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}+0,3	V
Output leakage current at V_O = V_{SS} to V_{DD}; OD = HIGH or chip disabled	$\|I_{OL}\|$	–	–	0,2	μA
Output voltage LOW at I_{OL} = 4,0 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 2,0 mA	V_{OH}	2,4	–	–	V

D.C. CHARACTERISTICS (V_{DD} = 3 V)

V_{DD} = 3 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	3,0	3,5	V
Operating supply current					
at V_I = V_{DD} or V_{SS}; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
at V_I = 0,4 or 1,6 V; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
Standby supply current at CE2 = V_{SS}	I_{SB}	–	0,02	5,0	μA
Input leakage current at V_I = V_{SS} to V_{DD}	$\|I_{IL}\|$	–	–	0,1	μA
Input voltage LOW	V_{IL}	−0,3	–	+0,4	V
Input voltage HIGH	V_{IH}	1,6	–	V_{DD}+0,3	V
Output leakage current at V_O = V_{SS} to V_{DD}; OD = HIGH or chip disabled	$\|I_{OL}\|$	–	–	0,2	μA
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,3	V
Output voltage HIGH at $-I_{OH}$ = 1,0 mA	V_{OH}	1,7	–	–	V

A.C. TEST CONDITIONS (V_{DD} = 5 V)

Input pulse levels	0,8 V to 2,0 V
Input rise and fall times	5 ns
Input timing reference levels	1,5 V
Output timing levels	1,5 V
Output timing levels for high/low impedance	1,2 V and 2,8 V
Output load (2 TTL inputs and load capacitance C_L)	Fig. 4

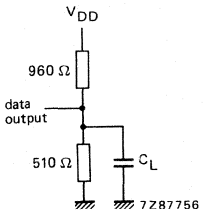


Fig. 4 Test load.

A.C. CHARACTERISTICS (V_{DD} = 5 V)

V_{DD} = 5 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; loads as per Fig. 4 with C_L = 100 pF unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	150	–	–	ns
Address access time	t_{AA}	–	–	150	ns
Chip enable $\overline{CE1}$ to output	t_{CO1}	–	–	150	ns
Chip enable CE2 to output	t_{CO2}	–	–	150	ns
Output disable OD to output	t_{OD}	–	–	70	ns
Data output to high impedance state at C_L = 5 pF	t_{DF}	10	–	70	ns
Previously read data valid with respect to address change	t_{OH1}	10	–	–	ns
Previously read data valid with respect to chip enable	t_{OH2}	10	–	–	ns
Write cycle					
Write cycle time	t_{WC}	150	–	–	ns
Write delay time	t_{AW}	0	–	–	ns
Chip enable $\overline{CE1}$ to write	t_{CW1}	120	–	–	ns
Chip enable CE2 to write	t_{CW2}	120	–	–	ns
Data set-up time	t_{DW}	70	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Write pulse duration	t_{WP}	70	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Output disable OD set-up time	t_{DS}	70	–	–	ns

A.C. TEST CONDITIONS (V_{DD} = 3 V)

Input pulse levels	0,4 V to 1,6 V
Input rise and fall times	5 ns
Input timing reference levels	1,0 V
Output timing levels	1,0 V
Output timing levels for high/low impedance	0,7 V and 1,7 V
Output load	Fig. 5

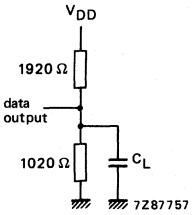


Fig. 5 Test load.

A.C. CHARACTERISTICS (V_{DD} = 3 V)

V_{DD} = 3 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; loads as per Fig. 5 with C_L = 100 pF unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	400	–	–	ns
Address access time	t_{AA}	–	–	400	ns
Chip enable $\overline{CE1}$ to output	t_{CO1}	–	–	400	ns
Chip enable CE2 to output	t_{CO2}	–	–	400	ns
Output disable OD to output	t_{OD}	–	–	200	ns
Data output to high impedance state at C_L = 5 pF	t_{DF}	10	–	200	ns
Previously read data valid with respect to address change	t_{OH1}	10	–	–	ns
Previously read data valid with respect to chip enable	t_{OH2}	10	–	–	ns
Write cycle					
Write cycle time	t_{WC}	400	–	–	ns
Write delay time	t_{AW}	0	–	–	ns
Chip enable $\overline{CE1}$ to write	t_{CW1}	300	–	–	ns
Chip enable CE2 to write	t_{CW2}	300	–	–	ns
Data set-up time	t_{DW}	200	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Write pulse duration	t_{WP}	200	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Output disable OD set-up time	t_{DS}	200	–	–	ns

WAVEFORMS

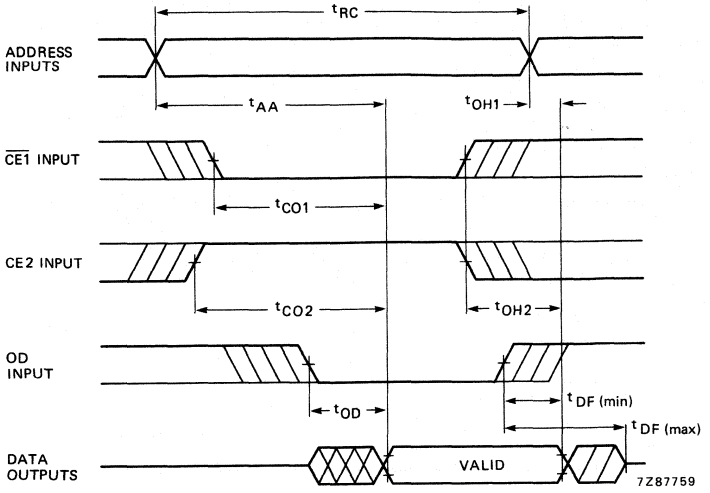


Fig. 6 Read cycle timing; R/$\overline{W}$ = HIGH.

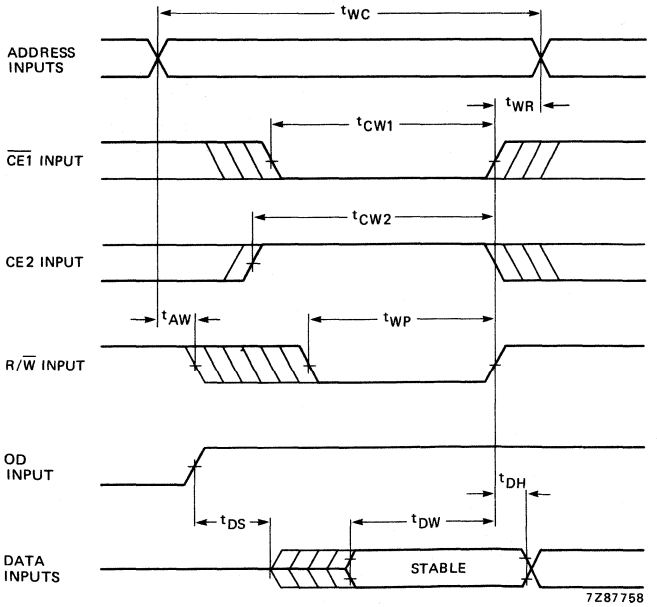


Fig. 7 Write cycle timing.

LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS

$CE2 \leqslant 0{,}2$ V; $T_{amb} = -25$ to $+70$ °C.

parameter	symbol	min.	typ.	max.	unit
Supply voltage for data retention	V_{DR}	1,0	–	5,5	V
Data retention current at V_{DD} = 1,5 V	I_{DR}	–	0,02	2,0	μA
Chip deselect to data retention time	t_{CDR}	0	–	–	ns
Operation recovery time	t_R	0	–	–	ns

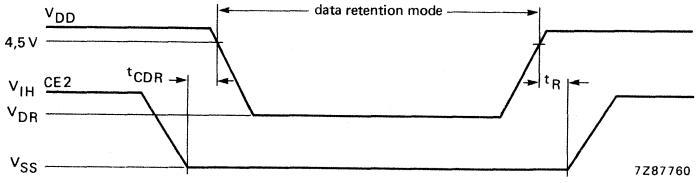


Fig. 8 Low supply voltage data retention characteristics.

1024 x 4-BIT STATIC RAM

GENERAL DESCRIPTION

The PCD5114 is a low-power, high-speed 4096-bit static CMOS RAM, organized as 1024 words of 4 bits each. The IC is suitable for low power and high speed applications, for battery operation and where battery backup is required. Inputs R/$\overline{W}$ and $\overline{CE}$ control the read/write operation and standby mode respectively. The PCD5114 is pin compatible with the SBB2114 types.

Features

• Operating supply voltage	2,5 V to 5,5 V
• Low data retention voltage	min. 1,0 V
• Low standby current	max. 10 μA
• Cycle time = access time	max. 200 ns

- Static operation requiring no clock or timing strobe
- Low power consumption
- 3-state common data input/output interface
- All inputs and outputs directly TTL compatible
- Pin compatible with SBB2114 variants
- 18-lead DIL package
- 20-lead SO package

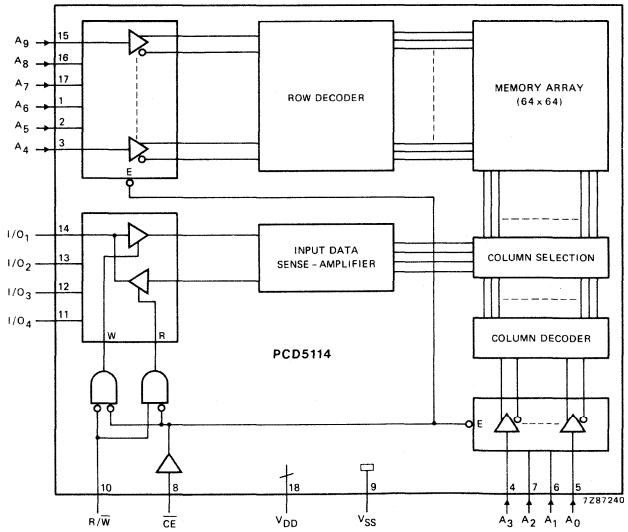


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCD5114D: 18-lead DIL; ceramic (cerdip) (SOT-133A,B).
PCD5114P: 18-lead DIL; plastic (SOT-102G).
PCD5114T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

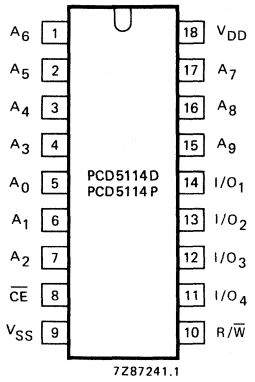


Fig. 2 Pinning diagram: PCD5114D; PCD5114P.

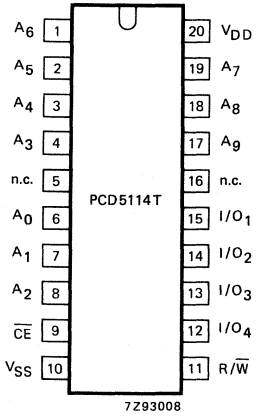


Fig. 3 Pinning diagram: PCD5114T.

A_0 to A_3	column inputs
A_4 to A_9	row address inputs
$\overline{CE}$	chip enable input
$R/\overline{W}$	read/write input
I/O_1 to I/O_4	data input/output
V_{SS}	negative supply (ground)
V_{DD}	positive supply (+ 5 V)

Table 1 Mode selection

$\overline{CE}$	$R/\overline{W}$	mode	output	power
H	H	not selected	high impedance	standby
H	L	not selected	high impedance	standby
L	H	read	active	active
L	L	write	high impedance	active

H = HIGH logic level (the most positive voltage)
L = LOW logic level (the most negative voltage)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to + 8 V
Input voltage range (any pin)	V_I	V_{SS}−0,3 to V_{DD} + 0,3 V
Storage temperature range	T_{stg}	−55 to + 125 °C
Operating ambient temperature range	T_{amb}	−25 to + 70 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DEVELOPMENT SAMPLE DATA

D.C. CHARACTERISTICS

V_{DD} = 5 V ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply current					
at $V_I = V_{DD}/V_{SS}$; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 V/2,0 V; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 V/2,0 V; f = 5 MHz; outputs open	I_{DD}	–	12	20	mA
Standby current					
at $\overline{CE} = V_{DD}$	I_{SB}	–	0,02	10	μA
Input voltage HIGH	V_{IH}	2,0	–	V_{DD} + 0,3	V
Input voltage LOW	V_{IL}	−0,3	–	+0,8	V
Input leakage current					
at $V_I = V_{SS}$ to V_{DD}	$\pm I_{IL}$	–	–	0,1	μA
Output voltage HIGH					
at $-I_{OH}$ = 2 mA	V_{OH}	2,4	–	–	V
Output voltage LOW					
at I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
Output leakage current					
at $V_O = V_{SS}$ to V_{DD}; $\overline{CE}$ = HIGH	$\pm I_{OL}$	–	–	0,5	μA

D.C. CHARACTERISTICS

V_{DD} = 3 V ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply current					
at $V_I = V_{DD}/V_{SS}$; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
at V_I = 0,4 V/1,6 V; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
Standby current					
at $\overline{CE} = V_{DD}$	I_{SB}	–	0,02	10	μA
Input voltage HIGH	V_{IH}	1,6	–	V_{DD} + 0,3	V
Input voltage LOW	V_{IL}	−0,3	–	+0,4	V
Input leakage current					
at $V_I = V_{SS}$ to V_{DD}	$\pm I_{IL}$	–	–	0,1	μA
Output voltage HIGH					
at $-I_{OH}$ = 1 mA	V_{OH}	1,7	–	–	V
Output voltage LOW					
at I_{OL} = 1 mA	V_{OL}	–	–	0,3	V
Output leakage current					
at $V_O = V_{SS}$ to V_{DD}; $\overline{CE}$ = HIGH	$\pm I_{OL}$	–	–	0,5	μA

A.C. CHARACTERISTICS

V_{DD} = 5 V ±0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; measured in Fig. 4, C_L = 100 pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	200	–	–	ns
Address access time	t_{AA}	–	–	200	ns
Chip select access time	t_{AC}	–	–	200	ns
Output hold from address change	t_{OHA}	20	–	–	ns
Output hold from chip select	t_{OHC}	20	–	–	ns
Output to low impedance from chip selection at C_L = 5 pF	t_{CLZ}	20	–	–	ns
Output to high impedance from chip deselection at C_L = 5 pF	t_{CHZ}	–	–	80	ns
Write cycle					
Write cycle time	t_{WC}	200	–	–	ns
Chip selection to end of write	t_{CW}	120	–	–	ns
Address set-up time	t_{AS}	0	–	–	ns
Write pulse duration	t_{WP}	140	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Data set-up time	t_{DS}	80	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Output to high impedance from write enabled at C_L = 5 pF	t_{WZ}	–	–	60	ns
Output active from end of write at C_L = 5 pF	t_{RZ}	20	–	–	ns

A.C. TEST CONDITIONS (see Fig. 4)

Input pulse levels	0,8 V to 2,0 V
Input rise and fall times	5 ns
Input timing reference levels	1,5 V
Output timing levels	1,5 V
Output timing levels for high/low impedance	1,2 V and 2,8 V
Output load	2 TTL gates and C_L = 100 pF

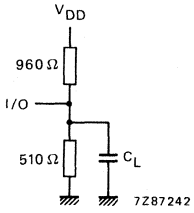


Fig. 4 Load for a.c. test conditions (V_{DD} = 5 V ± 0,5 V).

A.C. CHARACTERISTICS

V_{DD} = 3 V ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70°C; measured in Fig. 5, C_L = 100 pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	500	–	–	ns
Address access time	t_{AA}	–	–	500	ns
Chip select access time	t_{AC}	–	–	500	ns
Output hold from address change	t_{OHA}	20	–	–	ns
Output hold from chip select	t_{OHC}	20	–	–	ns
Output to low impedance from chip selection at C_L = 5 pF	t_{CLZ}	20	–	–	ns
Output to high impedance from chip deselection at C_L = 5 pF	t_{CHZ}	–	–	200	ns
Write cycle					
Write cycle time	t_{WC}	500	–	–	ns
Chip selection to end of write	t_{CW}	300	–	–	ns
Adress set-up time	t_{AS}	0	–	–	ns
Write pulse duration	t_{WP}	350	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Data set-up time	t_{DS}	200	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Output to high impedance from write enabled at C_L = 5 pF	t_{WZ}	–	–	150	ns
Output active from end of write at C_L = 5 pF	t_{RZ}	20	–	–	ns

DEVELOPMENT SAMPLE DATA

A.C. TEST CONDITIONS (see Fig. 5)

Input pulse levels	0,4 V to 1,6 V
Input rise and fall times	5 ns
Input timing reference levels	1,0 V
Output timing levels	1,0 V
Output timing levels for high/low impedance	0,7 V and 1,7 V
Output load	2 TTL gates and C_L = 100 pF

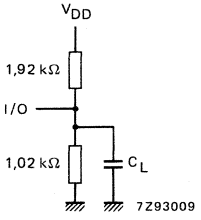


Fig. 4 Load for a.c. test conditions (V_{DD} = 5 V ± 0,5 V).

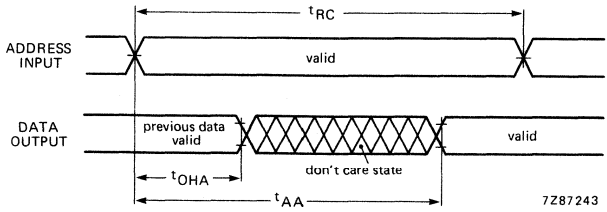


Fig. 6 Read cycle timing (1): R/$\overline{W}$ is HIGH; $\overline{CE}$ is LOW for a read cycle.

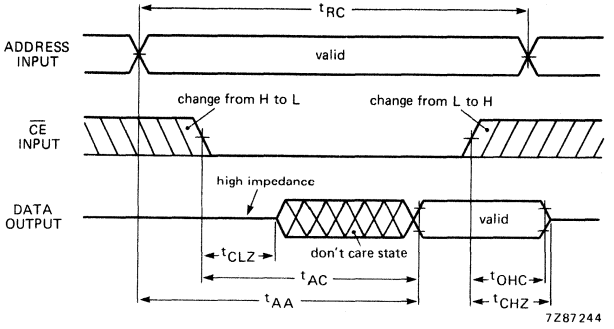


Fig. 7 Read cycle timing (2): R/$\overline{W}$ is HIGH for a read cycle.

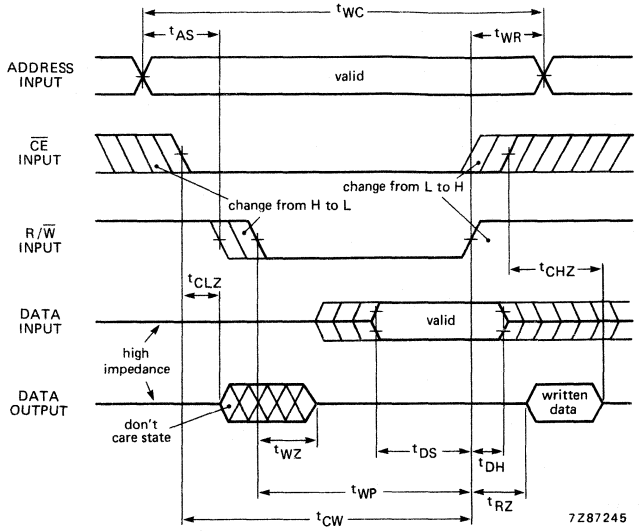


Fig. 8 Write cycle (1): R/$\overline{W}$ controlled.

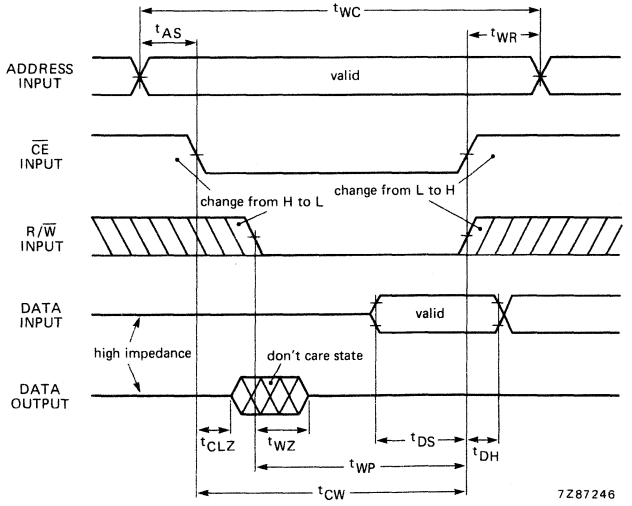


Fig. 9 Write cycle (2): $\overline{CE}$ controlled.

Note : If the $\overline{CE}$ low transition occurs after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.

CAPACITANCE

$f = 1$ MHz; $T_{amb} = 25\ ^{o}C$

parameter	symbol	min.	typ.	max.	unit
Input capacitance at $V_I = V_{SS}$	C_I	–	–	5	pF
Output capacitance at $V_O = V_{SS}$	C_O	–	–	5	pF

LOW V_{DD} DATA RETENTION CHARACTERISTICS

$T_{amb} = -25$ to $+70\ ^{o}C$

parameter	symbol	min.	typ.	max.	unit
V_{DD} for data retention at $\overline{CE} = V_{DDR} \pm 0{,}2$ V; $V_I = V_{DDR}$ or V_{SS}	V_{DDR}	1	–	5,5	V
Data retention current at $V_{DDR} = 1{,}5$ V	I_{DDR}	–	0,02	5	μA
Chip deselect to data retention time	t_{CR}	0	–	–	ns
Operation recovery time	t_R	0	–	–	ns

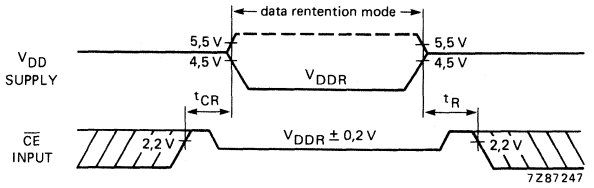


Fig. 10 LOW V_{DD} data retention.

128 x 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCD8571 is a low power 1024-bit static CMOS RAM organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1, A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 5 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I^2C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3340 applications)
- Radio and television — channel presets
- Video cassette recorder
- General purpose — RAM expansion for the microcomputer families MAB8400 and PCF84C00

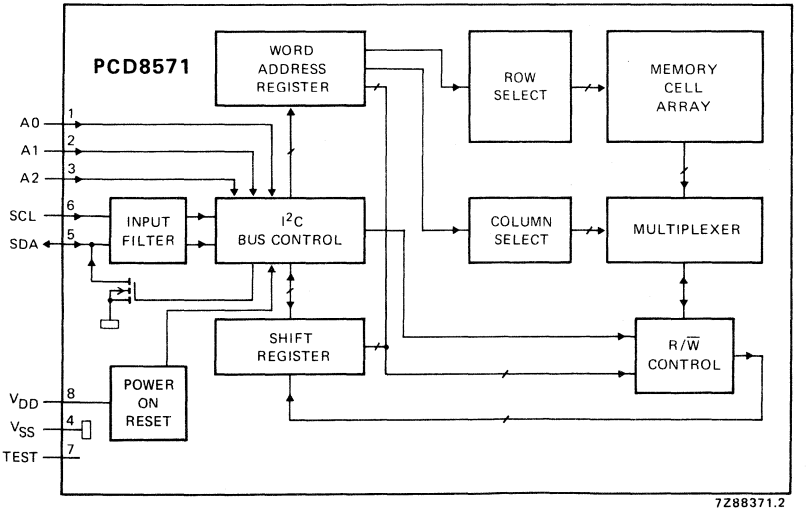


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCD8571P: 8-lead DIL; plastic (SOT-97A).
PCD8571D: 8-lead DIL; ceramic (cerdip) (SOT-151A).
PCD8571T: 8-lead mini-pack (SO-8L; SOT-176).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line } I^2C bus
6	SCL	serial clock line } I^2C bus
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Fig. 14 and 15)
8	V_{DD}	positive supply

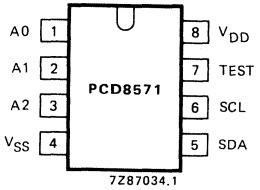


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V_{DD}	−0,8 to + 8,0	V
Voltage range on any input	V_I	−0,8 to V_{DD} + 0,8	V
D.C. input current (any input)	$\pm I_I$	max. 10	mA
D.C. output current (any output)	$\pm I_O$	max. 10	mA
Supply current (pin 4 or pin 8)	$\pm I_{DD}; I_{SS}$	max. 50	mA
Power dissipation per package	P_{tot}	max. 300	mW
Power dissipation per output	P	max. 50	mW
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating temperature range	T_{amb}	−25 to + 70	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current at f_{SCL} = 100 kHz $V_I = V_{SS}$ or V_{DD}					
operating	I_{DD}	–	–	200	μA
standby	I_{DDO}	–	–	5	μA
Power-on reset voltage level* at $V_{SCL} = V_{SDA} = V_{DD}$	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW**	V_{IL}	−0,8	–	0,3 x V_{DD}	V
Input voltage HIGH**	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	100	nA
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\pm I_I$	–	–	100	nA
Clock frequency (Fig. 7)	f_{SCL}	0	–	100	kHz
Input capacitance (SCL, SDA) at $V_I = V_{SS}$	C_I	–	–	7	pF
Tolerable spike width on bus	t_{SW}	–	–	100	ns
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V	I_{DDR}	–	–	2	μA
Power saving mode (Fig. 14)					
Supply current at T_{amb} = 25 °C; TEST = A0 = A1 = A2 = V_{DDR}	I_{DDS}	–	50	200	nA

* The power-on reset circuit resets the I²C bus logic when $V_{DD} < V_{POR}$.

** If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow: this current must not exceed ± 0,5 mA.

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

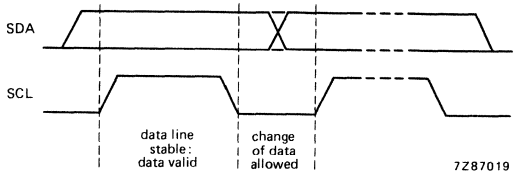


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

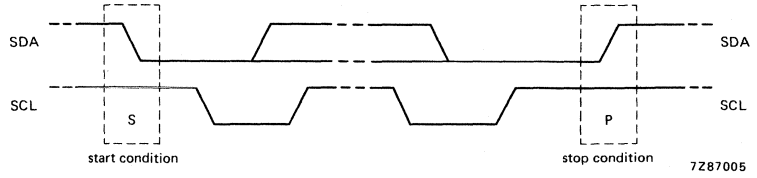


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

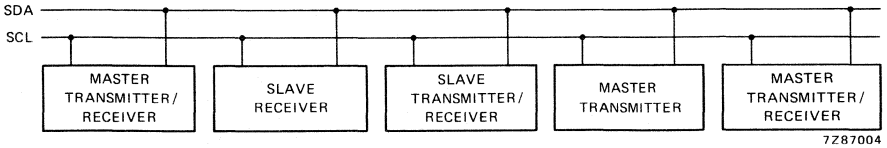


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

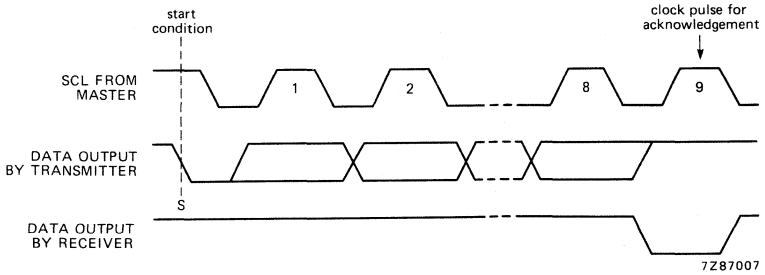


Fig. 6 Acknowledgement on the I^2C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCD8571 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

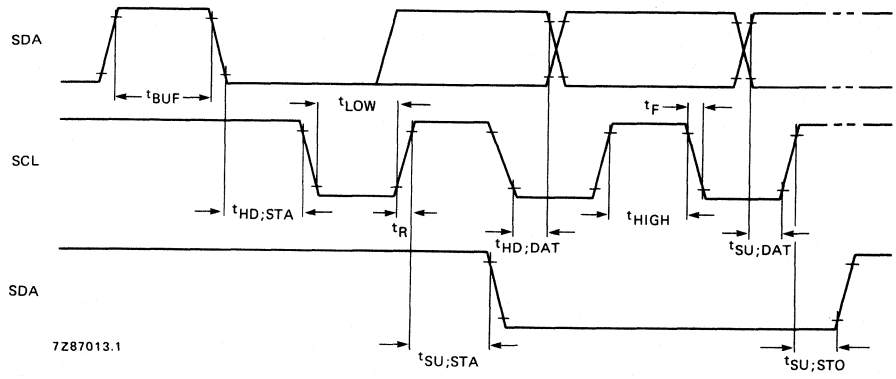


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

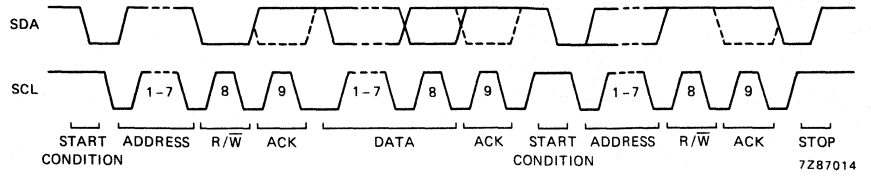


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

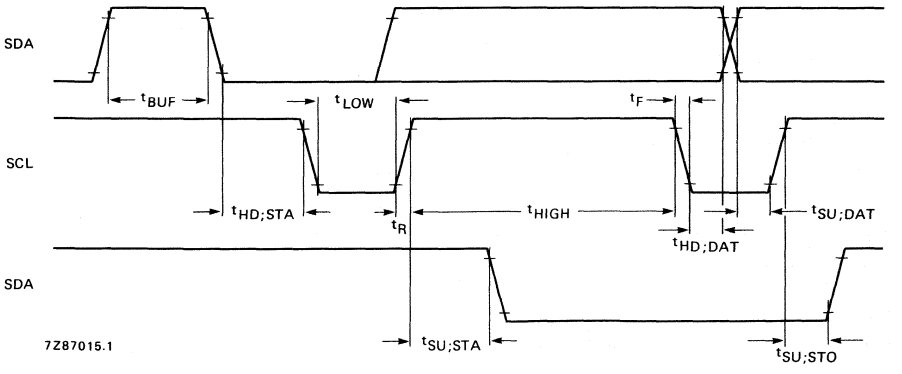


Fig. 9 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

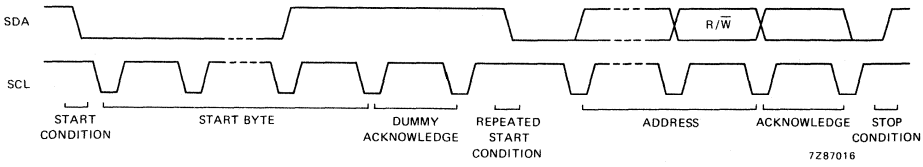


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

Bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCD8571 READ and WRITE cycles is shown in Fig. 11.

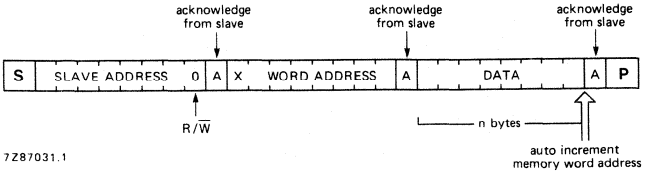


Fig. 11(a) Master transmits to slave receiver (WRITE mode).

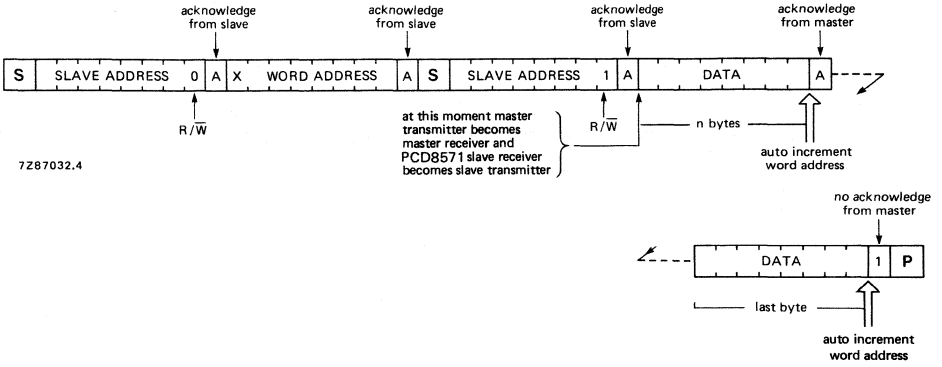


Fig. 11(b) Master reads after setting word address (WRITE word address; READ data).

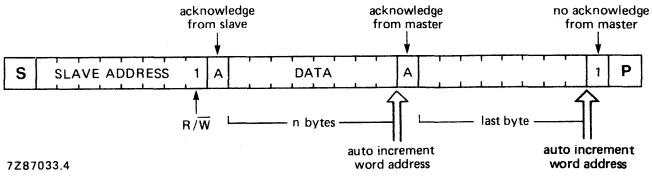


Fig. 11(c) Master reads slave immediately after first byte (READ mode).

Note

X = don't care bit.

APPLICATION INFORMATION

The PCD8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 12).

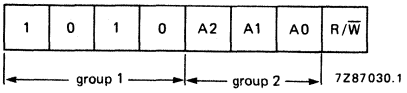


Fig. 12 PCD8571 address.

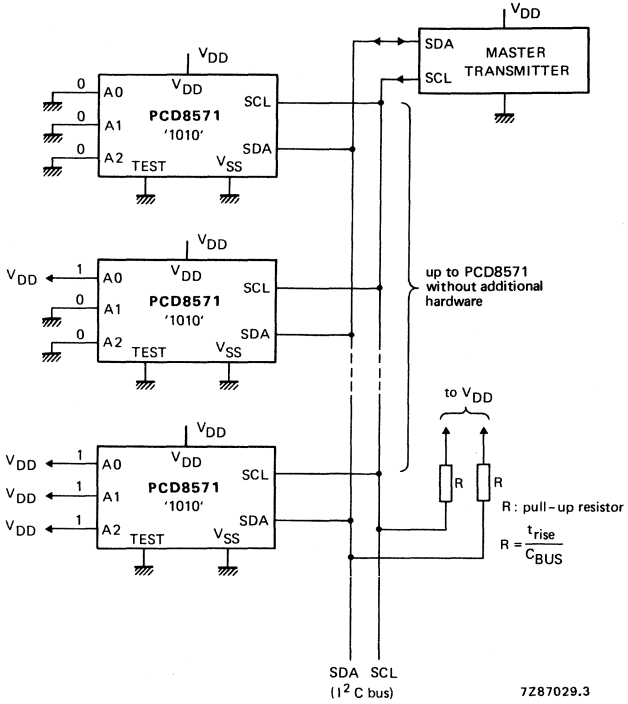


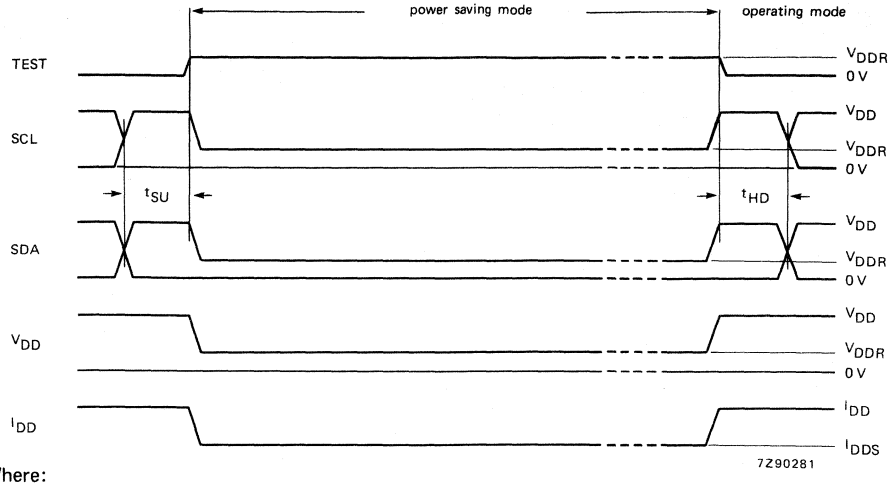
Fig. 13 PCD8571 application diagram.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open.

POWER SAVING MODE

With the condition TEST = A2 = A1 = A0 = V_{DDR}, the PCD8571 goes into the power saving mode.



Where:
$t_{SU} \geqslant 4\ \mu s$
$t_{HD} \geqslant 4\ \mu s$

Fig. 14 Timing for power saving mode.

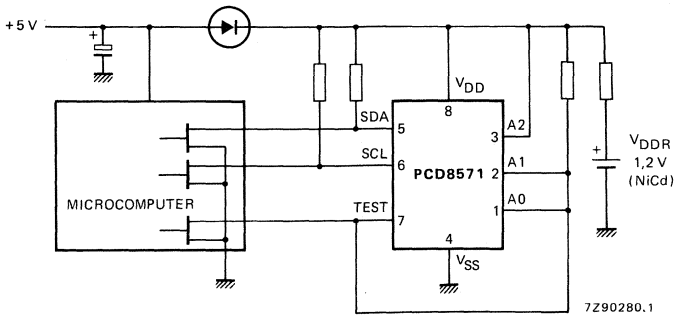


Fig. 15 Application example for power saving mode.

Note

1. In the operating mode, TEST = 0 (A0, A1 = 0; A2 = 1).
2. In the power saving mode, TEST = A0 = A1 = A2 = V_{DDR}.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

MICROPOWER VOLTAGE DETECTOR

GENERAL DESCRIPTION

The PCF1251 is a CMOS micropower voltage detector and it is especially designed for power-on/off voltage detection monitoring and reset. The IC has an extremely low current consumption and is therefore particularly suited for battery operated applications. The internal bandgap reference voltage is stable with temperature variations. The voltage trip-point and the hysteresis can be set independently with external resistors. Two of the four outputs can be delayed with an external capacitor.

Features

- Extremely low current consumption
- Built-in bandgap voltage reference
- Wide range of voltage trip-points
- Two pairs of outputs; one pair with delay possibility
- 8-lead DIL or SO-8 mini-pack (plastic packages)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range with respect to V_{SS}	V_{DD}	1	–	6	V
Supply current	I_{DD}	–	1	–	μA
Output currents at V_{DD} = 1 V	I_O	–	2	–	mA
Bandgap voltage reference	V_{REF}	1,0	1,15	1,3	V

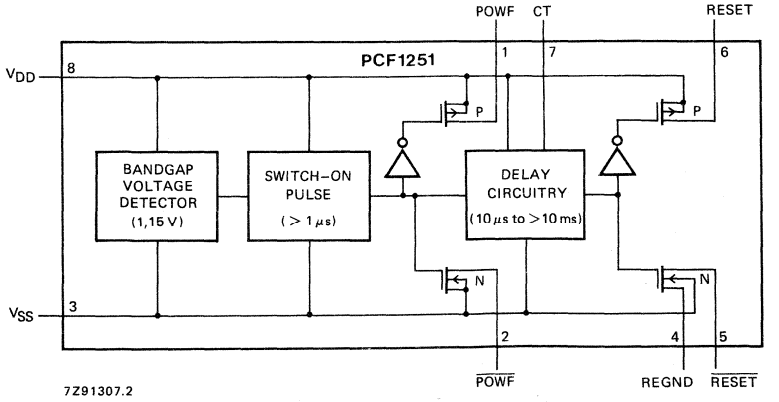


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF1251P: 8-lead DIL; plastic (SOT-97A).
PCF1251T: 8-lead mini-pack; plastic (SO-8; SOT-96A).

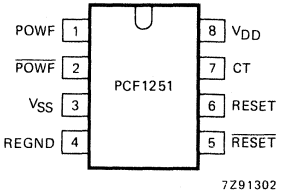


Fig. 2 Pinning diagram.

PINNING

1	POWF	power-fail output
2	$\overline{\text{POWF}}$	power-fail output (inverted)
3	V_{SS}	negative supply voltage
4	REGND	reset ground
5	$\overline{\text{RESET}}$	reset output (inverted; delayed)
6	RESET	reset output (delayed)
7	CT	capacitor for additional delay
8	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

The PCF1251 consists of a bandgap voltage reference, a comparator and delay circuitry (see Fig. 1). The supply voltage of the circuit (V_{DD} with respect to V_{SS}) is compared with an internal bandgap voltage reference by means of a special comparator. This comparator is connected to the circuit supply voltage. As long as the supply voltage is above the reference voltage level, the four open-drain outputs are all switched off and an extended drain-source voltage of up to 6 V is allowed. When the supply voltage is reduced and reaches the reference voltage level (V_{REF}), the power-fail outputs are switched on (p-channel for POWF and n-channel for $\overline{\text{POWF}}$ outputs). After a delay, determined by an external capacitor between pins CT and V_{DD}, the outputs RESET and $\overline{\text{RESET}}$ are switched on. The same delay will be active when the supply voltage is increased again and exceeds the internal voltage reference, resulting in switching off the outputs.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage with respect to V_{SS}	V_{DD}	–	8	V
Output voltage at pin 2 V_{DD} with respect to V_2	V_2	–	8	V
Output voltage at pin 5 (pin 4 at V_{SS}) V_{DD} with respect to V_5	V_5	–	8	V
Output voltage at pin 1 V_1 with respect to V_{SS}	V_1	–	8	V
Output voltage at pin 6 V_6 with respect to V_{SS}	V_6	–	8	V
Voltage at pin 7 (CT)	V_7	−0,5	V_{DD} + 0,5	V
Current at pin 7 (CT)	I_7	–	20	mA
Output currents at pins 1, 2, 5 and 6	$\lvert I_O \rvert$	–	25	mA
Total power dissipation	P_{tot}	–	150	mW
Operating ambient temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−55	+125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 1 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	1	–	6	V
Operating supply current V_{DD} = 6 V; all outputs open	I_{DD}	–	1	3	μA
Bandgap voltage reference	V_{REF}	1,0	1,15	1,3	V
Output current at pins 2 and 5 T_{amb} = 25 °C; $V_{DD} < V_{REF}$; V_O = 0,4 V with respect to V_{SS}	I_O	1	2	–	mA
Output current at pins 1 and 6 T_{amb} = 25 °C; $V_{DD} < V_{REF}$; $-V_O$ = 0,4 V with respect to V_{DD}	$-I_O$	1	2	–	mA

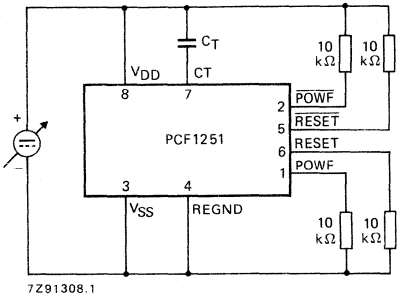


Fig. 3 Test circuit for timing measurements.

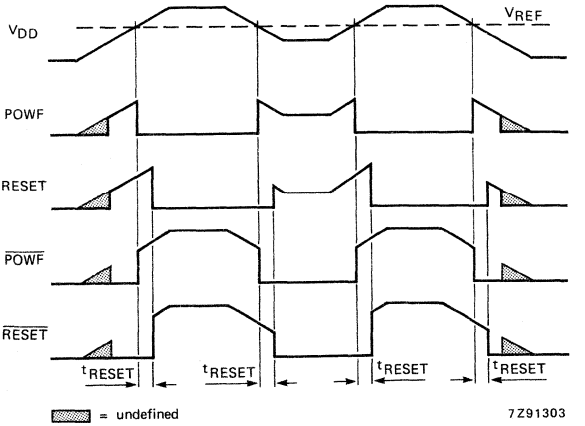


Fig. 4 Timing diagram for slow supply voltage changes.

(1) $t_{RESET} = 3{,}2\ ms^{+75\%}_{-50\%} \times C_T\ (nF)$

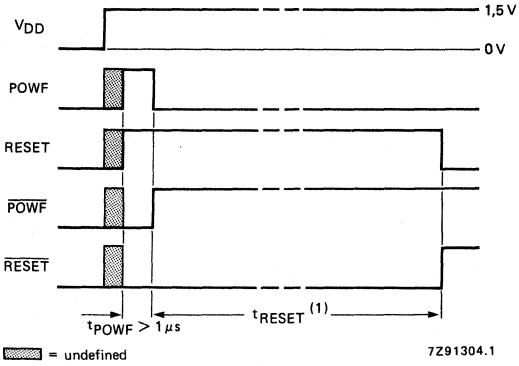


Fig. 5 Timing diagram for fast supply voltage switching on.

APPLICATION INFORMATION

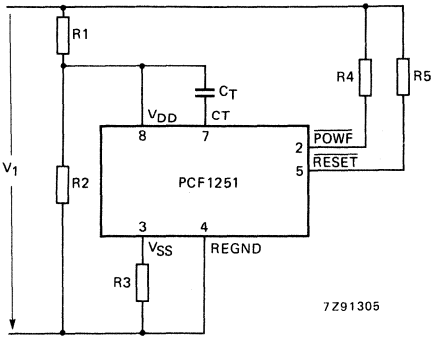


Fig. 6 Application circuit diagram.

(1) $V_{HYST} = V_1 \times \frac{R3}{R3 + R4}$; (0,4 V max.)

(2) $V_{TRIP} = V_{REF} \times \frac{R1 + R2}{R2}$

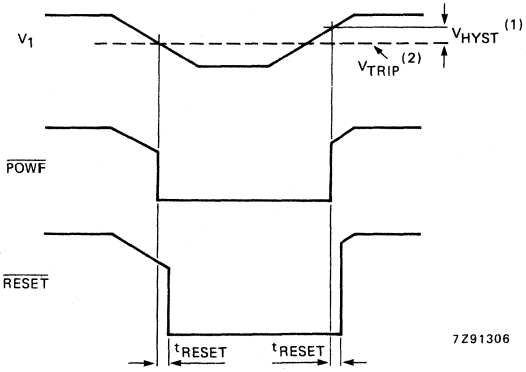


Fig. 7 Timing diagram for the circuit of Fig. 6.

LCD DUPLEX DRIVER

GENERAL DESCRIPTION

The PCF2111 is a single chip, silicon gate CMOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 64 segments in a duplex manner; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- 64 LCD-segment drive capability
- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possiblity

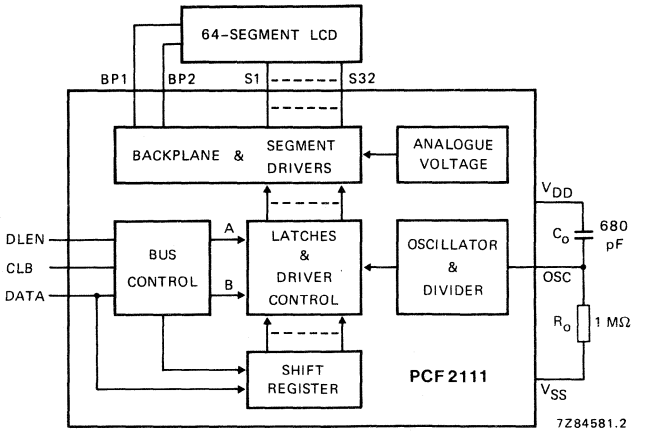


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF2111P: 40-lead DIL; plastic (SOT-129).
PCF2111T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS}	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_n	V_{SS} −0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−40 to + 85 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,25 to 6,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; R_o = 1 MΩ; C_o = 680 pF; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply current	no external load	I_{DD}	–	10	50	μA
Supply current	no external load; T_{amb} = −25 to + 85 °C	I_{DD}	–	–	30	μA
Display frequency	see Fig. 8; T = 680 μs	f_{LCD}	60	80	100	Hz
D.C. component of LCD drive	with respect to V_{SX}	V_{BP}	–	± 10	–	mV
Load on each segment driver			–	–	10	MΩ
			–	–	500	pF
Load on each backplane driver			–	–	1	MΩ
			–	–	5	nF
Input voltage HIGH	see Fig. 9	V_{IH}	2	–	–	V
Input voltage LOW	see Fig. 9	V_{IL}	–	–	0,6	V
Rise time V_{BP} to V_{SX}	max. load	t_r	–	20	–	μs
Inputs CLB, DATA, DLEN	see note on next page					
Input capacitance	for SOT-129 package	C_{IN}	–	–	10	pF
	for SOT-158A package	C_{IN}	–	–	5	pF
Rise and fall times	see Fig. 2	t_r, t_f	–	–	10	μs
CLB pulse width HIGH	see Fig. 2	t_{WH}	1	–	–	μs
CLB pulse width LOW	see Fig. 2	t_{WL}	9	–	–	μs

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
Data set-up time DATA → CLB	see Fig. 2	t_{SUDA}	8	–	–	μs
Data hold time DATA → CLB	see Fig. 2	t_{HDDA}	8	–	–	μs
Enable set-up time DLEN → CLB	see Fig. 2	t_{SUEN}	1	–	–	μs
Disable set-up time CLB → DLEN	see Fig. 2	t_{SUDI}	8	–	–	μs
Set-up time (load pulse) DLEN → CLB	see Fig. 2	t_{SULD}	8	–	–	μs
Busy-time from load pulse to next start of transmission	see Fig. 2	t_{BUSY}	8	–	–	μs
Set-up time (leading zero) DATA → CLB	see Fig. 2	t_{SULZ}	8	–	–	μs

Note

All timing values are referred to $V_{IH\ min}$ and $V_{IL\ max}$* (see Fig. 2). If external resistors are used in the bus lines (see Fig. 9), the extra time constant has to be added.

* With an input voltage swing of $V_{IL\ max}$–0,1 V to V_{IHmin} + 0,1 V.

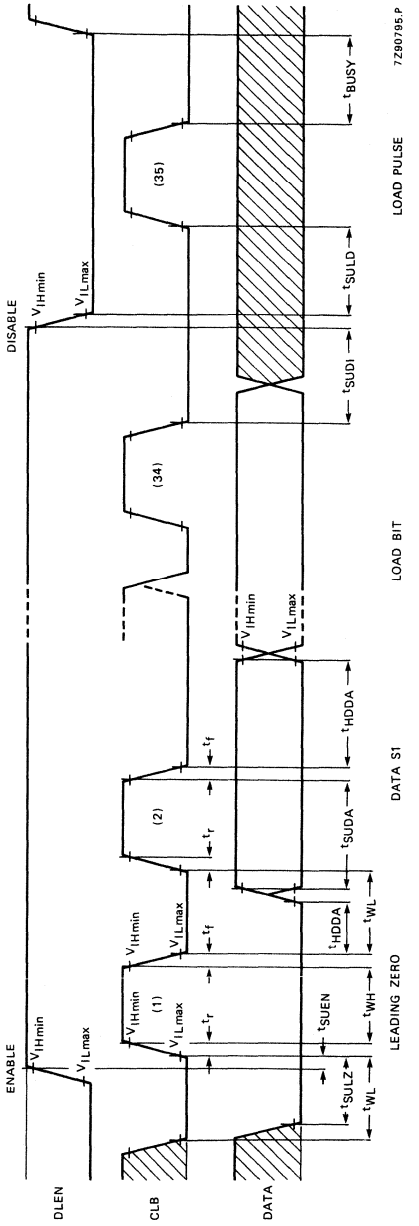


Fig. 2 CBUS timing.

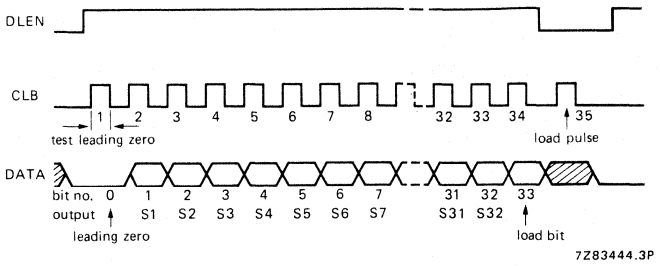


Fig. 3 CBUS data format.

Notes to Fig. 3

An LCD segment is activated when the corresponding DATA-bit is HIGH.
When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 33 LOW, the B-latches (BP2) are loaded. CLB-pulse 35 transfers data from shift register to selected latches.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN is LOW) and the driver is ready to receive new data.

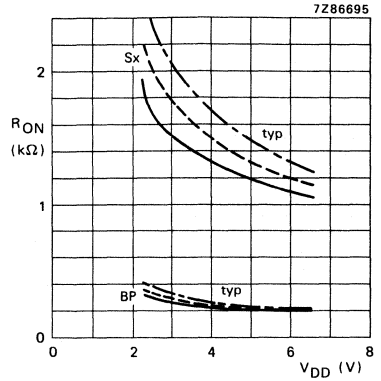


Fig. 4 Output resistance of backplane and segments.
——— T_{amb} = −40 °C; − − − T_{amb} = + 25 °C; — · — · T_{amb} = +85 °C.

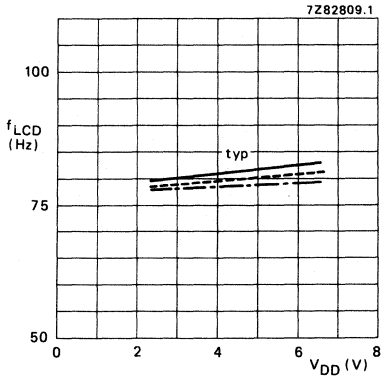


Fig. 5 Display frequency as a function of supply voltage; R_oC_o = 680 μs.
——— T_{amb} = −40 °C; − − − T_{amb} = + 25 °C; — · — · T_{amb} = +85 °C.

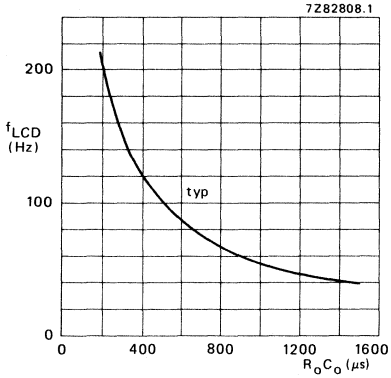


Fig. 6 Display frequency as a function of R_o x C_o time; T_{amb} = 25 °C.

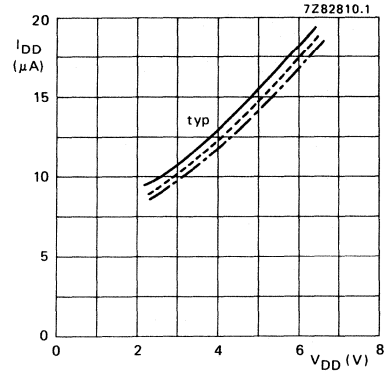


Fig. 7 Supply current as a function of supply voltage.
——— T_{amb} = −40 °C; − − − T_{amb} = + 25 °C; — · — · T_{amb} = +85 °C.

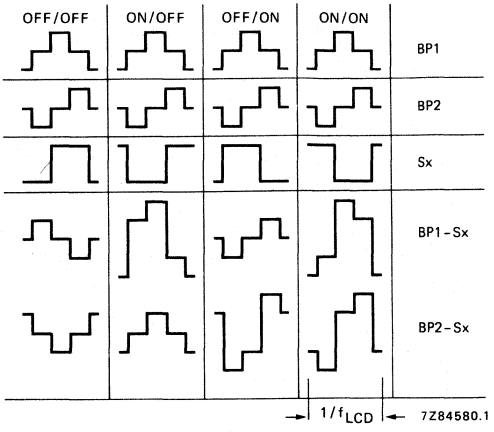


Fig. 8 Timing diagram.

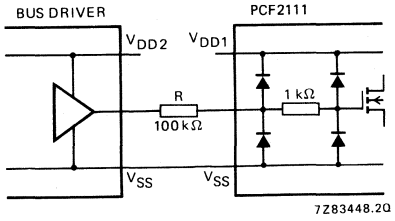
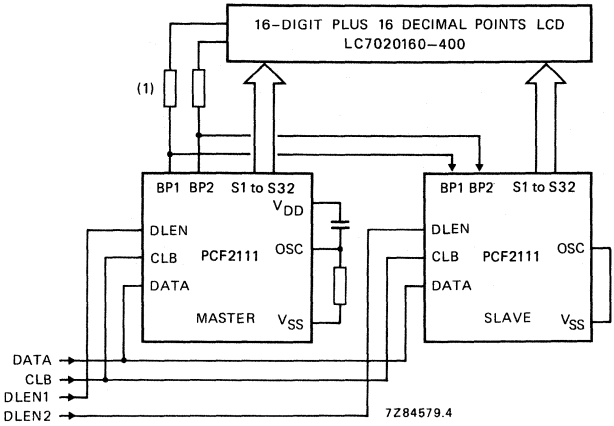


Fig. 9 Input circuitry.

Note to Fig. 9

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection.
Maximum input current $\leqslant$ 40 μA.



(1) In the slave mode, the serial resistors between BP1 and BP2 of the PCF2111 and the backplane of the LCD must be $> 2{,}7$ kΩ. In most applications the resistance of the interconnection to the LCD already has a higher value.

Fig. 10 Diagram showing expansion possibility for a 16-digit plus 16 decimal points LCD.

Note to Fig. 10

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several PCF2111, PCF2110 and PCF2100 ICs up to the BP drive capability of the master.

PCF2100 is a 40 LCD-segment driver; PCF2110 is a 60 LCD-segment driver plus 2 LED driver outputs.

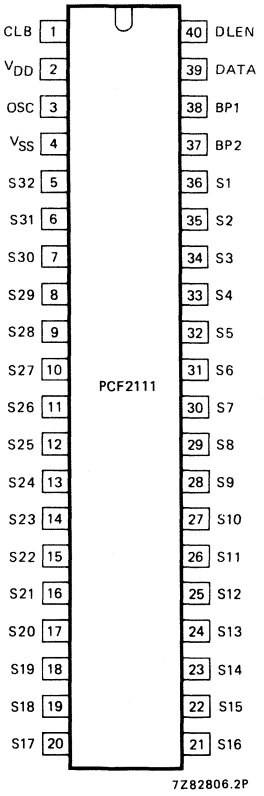


Fig. 11 Pinning diagram.

PINNING

Supply

2	V_{DD}	Positive supply
4	V_{SS}	Negative supply

Inputs

3	OSC	Oscillator input	
39	DATA	Data line	CBUS
40	DLEN	Data line enable	CBUS
1	CLB	Clock burst	CBUS

Outputs

38	BP1	Backplane drivers (common of LCD)
37	BP2	Backplane drivers (common of LCD)
S1 to S32		LCD driver outputs

256 x 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCF8570 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1, A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I^2C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony
- Radio and television
- Video cassette recorder
- General purpose

RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
channel presets

RAM expansion for the microcontroller families MAB8400 and PCF84C00

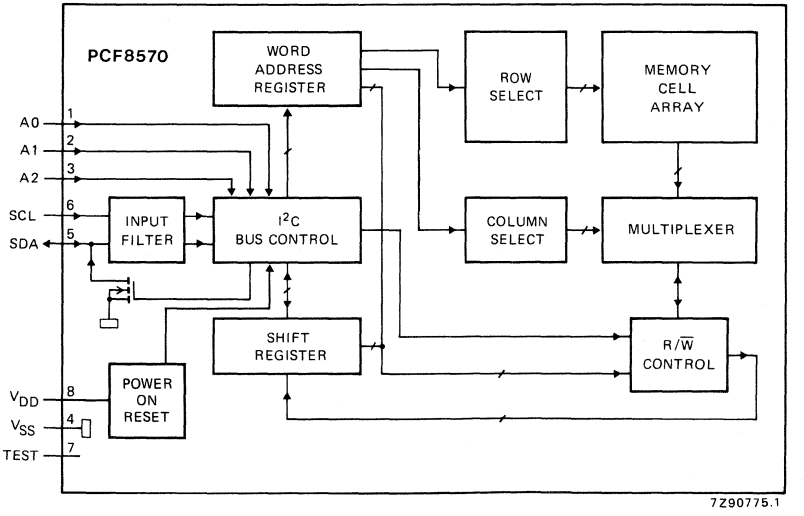


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8570P: 8-lead DIL; plastic (SOT-97A).
PCF8570T: 8-lead mini-pack plastic (SO-8L; SOT-176).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line (I²C bus)
6	SCL	serial clock line (I²C bus)
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 14 and 15)
8	V_{DD}	positive supply

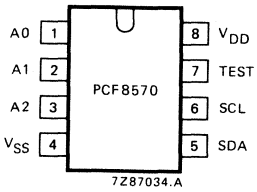


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V_{DD}	−0,8 to + 8,0	V
Voltage range on any input	V_I	−0,8 to V_{DD} + 0,8	V
D.C. input current (any input)	$\pm I_I$	max. 10	mA
D.C. output current (any output)	$\pm I_O$	max. 10	mA
Supply current (pin 4 or pin 8)	$\pm I_{DD}$; I_{SS}	max. 50	mA
Power dissipation per package	P_{tot}	max. 300	mW
Power dissipation per output	P	max. 50	mW
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	−40 to + 85	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current at $V_I = V_{SS}$ or V_{DD}					
operating at f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
standby at f_{SCL} = 0 Hz	I_{DDO}	–	–	15	μA
standby at T_{amb} = −25 to + 70 °C	I_{DDO}	–	–	5	μA
Power-on reset voltage level*	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW**	V_{IL}	−0,8	–	0,3 x V_{DD}	V
Input voltage HIGH**	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\pm I_I$	–	–	250	nA
Clock frequency (Fig. 7)	f_{SCL}	0	–	100	kHz
Input capacitance (SCL, SDA) at $V_I = V_{SS}$	C_I	–	–	7	pF
Tolerable spike width on bus	t_{SW}	–	–	100	ns
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
Supply current at V_{DDR} = 1 V; T_{amb} = −25 to + 70 °C	I_{DDR}	–	–	2	μA
Power saving mode (Figs 14 and 15)					
Supply current at T_{amb} = 25 °C; TEST = V_{DDR}	I_{DDR}	–	50	400	nA

* The power-on reset circuit resets the I^2C bus logic when $V_{DD} < V_{POR}$.

** If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ± 0,5 mA.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

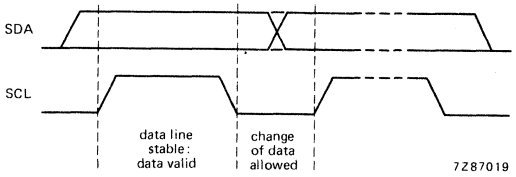


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

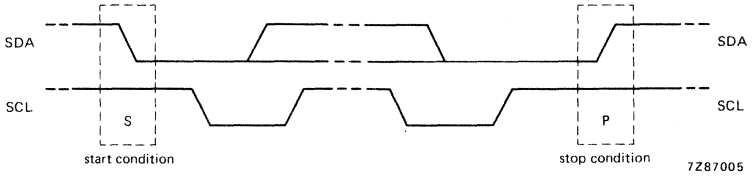


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

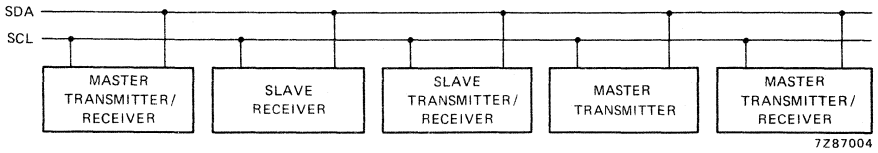


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

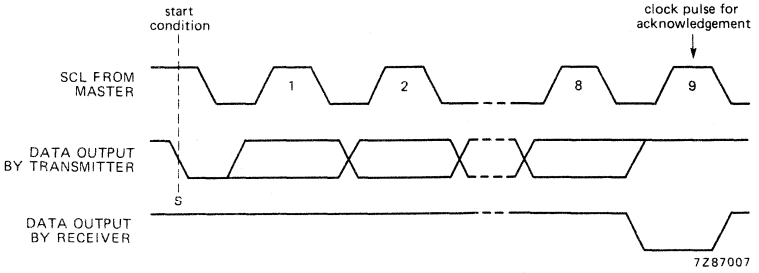


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

Within the I^2C bus specifications a high-speed mode and a low-speed mode are defined. The device operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

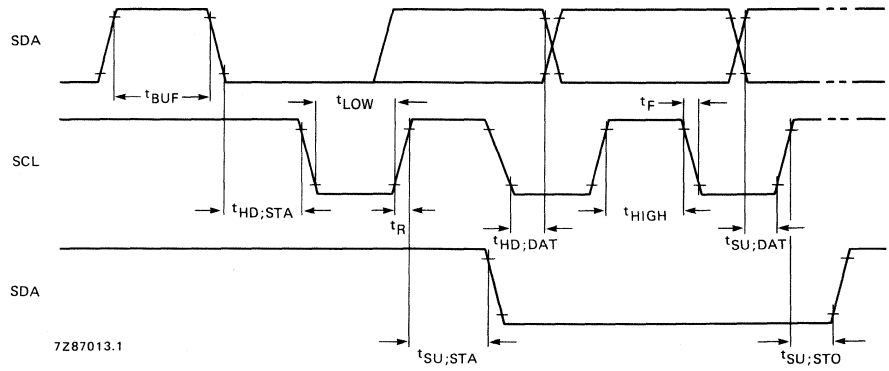


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

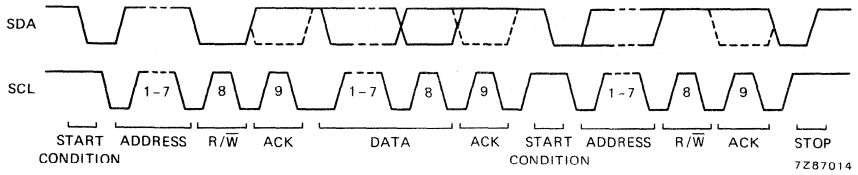


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

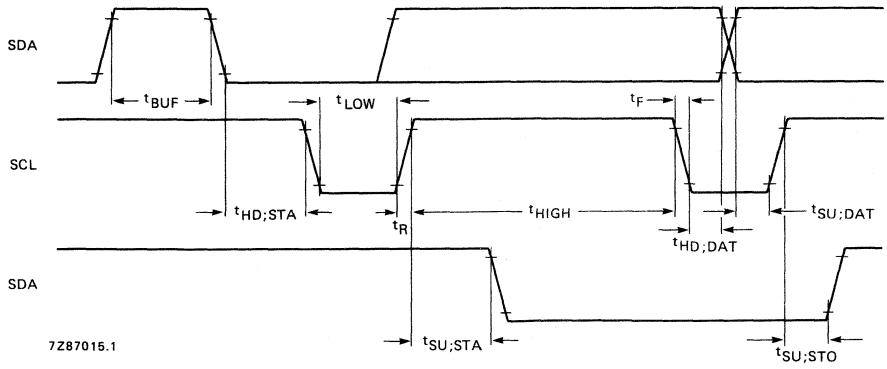


Fig. 9 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

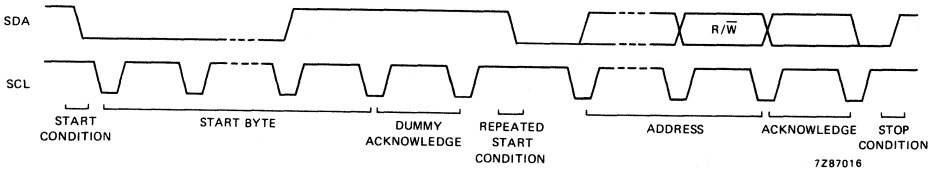


Fig. 10 Complete data transfer in the low-speed mode.

Where:	
Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

Bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCF8570 READ and WRITE cycles is shown in Fig. 11.

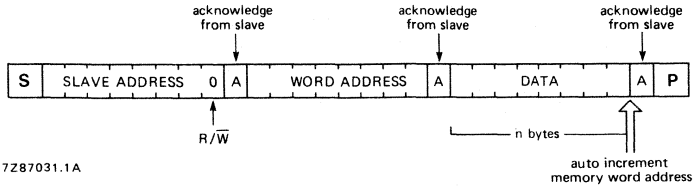


Fig. 11(a) Master transmits to slave receiver (WRITE mode).

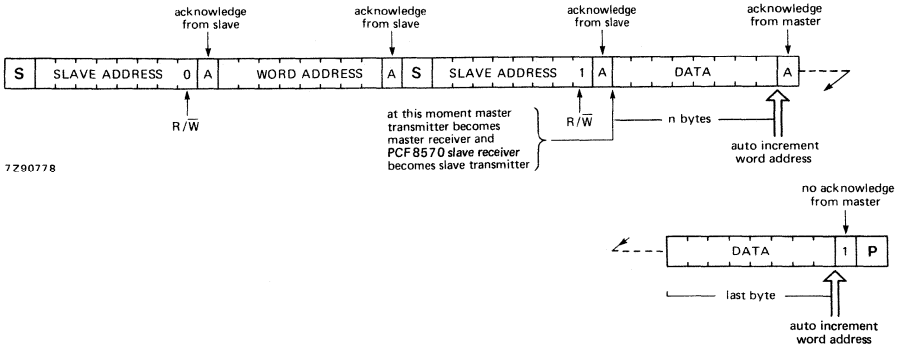


Fig. 11(b) Master reads after setting word address (WRITE word address; READ data).

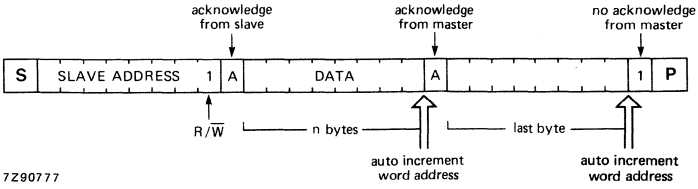


Fig. 11(c) Master reads slave immediately after first byte (READ mode).

APPLICATION INFORMATION

The PCF8570 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 12).

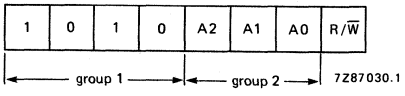


Fig. 12 PCF8570 address.

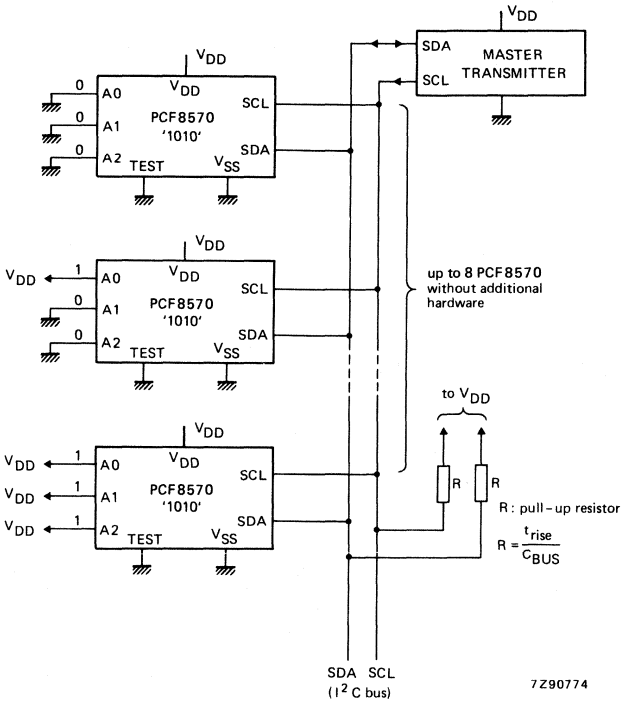


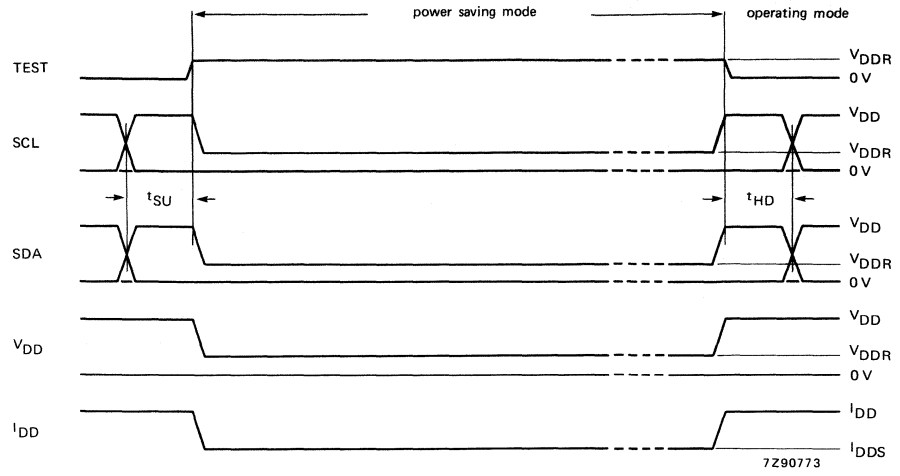
Fig. 13 PCF8570 application diagram.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open.

POWER SAVING MODE

With the condition TEST = V_{DDR}, the PCF8570 goes into the power saving mode and the I^2C bus logic is reset.



Where:
$t_{SU} \geqslant 4\ \mu s$
$t_{HD} \geqslant 4\ \mu s$

Fig. 14 Timing for power saving mode.

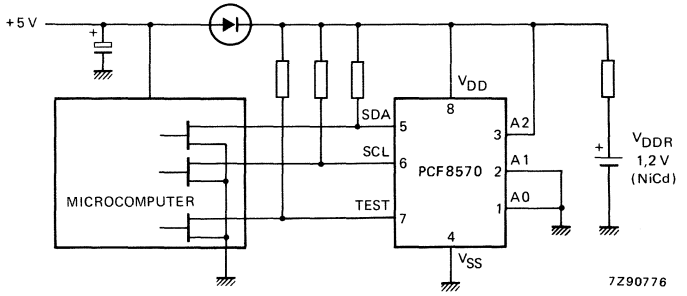


Fig. 15 Application example for power saving mode.

Note to Fig. 15

1. In the operating mode, TEST = 0.
2. In the power saving mode, TEST = V_{DDR}.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specification defined by Philips.

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, monolithic CMOS circuit that functions as a real time clock/calendar in the Inter IC (I^2C) bus-oriented microcomputer systems. The device includes an addressable time counter and an addressable alarm register, both for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred serially via a two line bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1,2 V nickel cadmium battery. The time base is generated from a 32,768 kHz crystal-controlled oscillator.

Features

- Serial input/output bus (I^2C) interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32,768 kHz)

QUICK REFERENCE DATA

Supply voltage range (clock)	$V_{DD}-V_{SS1}$		1,1 to 6,0 V
Supply voltage range (I^2C interface)	$V_{DD}-V_{SS2}$		2,5 to 6,0 V
Crystal oscillator frequency	f_{osc}	typ.	32,768 kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT-38).
PCF8573T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

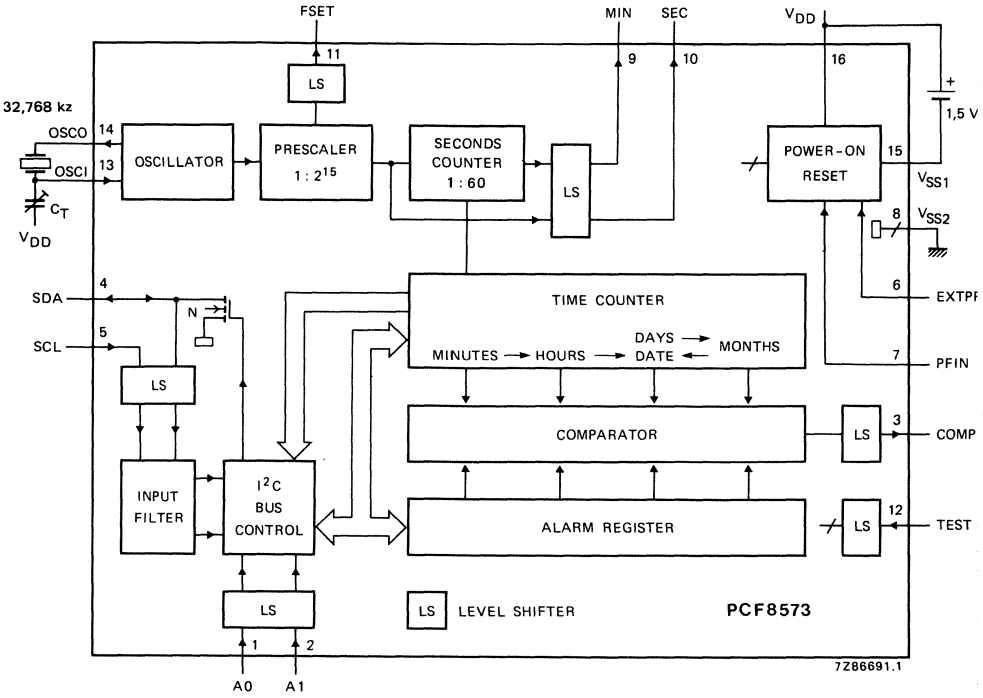


Fig. 1 Block diagram.

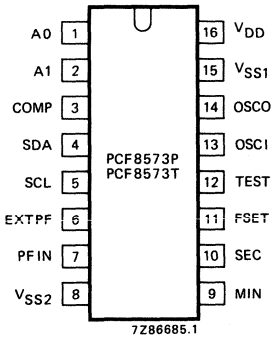


Fig. 2 Pinning diagram.

PINNING

1	A0	address input	
2	A1	address input	
3	COMP	comparator output	
4	SDA	serial data line	I^2C bus
5	SCL	serial clock line	I^2C bus
6	EXTPF	enable power fail flag input	
7	PFIN	power fail flag input	
8	V_{SS2}	negative supply 2 (I^2C interface)	
9	MIN	one pulse per minute output	
10	SEC	one pulse per second output	
11	FSET	oscillator tuning output	
12	TEST	test input; must be connected to V_{SS2} when not in use	
13	OSCI	oscillator input	
14	OSCO	oscillator input/output	
15	V_{SS1}	negative supply 1 (clock)	
16	V_{DD}	common positive supply	

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32,768 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I^2C bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH to LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (see note)
			or 29 → 01	
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note: Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I^2C bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I^2C bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I^2C bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I^2C bus.

FUNCTIONAL DESCRIPTION (continued)

Power on/power fail detection

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD}-V_{SS1}$) greater than V_{TH1}, or by an externally generated power fail signal for application with ($V_{DD}-V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

0 : connected to V_{SS1} (LOW)
1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C bus. A power on reset for the I^2C bus control is generated on-chip when the supply voltage $V_{DD}-V_{SS2}$ is less than V_{TH2}.

Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD}-V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD}-V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{SS2} = V_{DD}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig. 3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

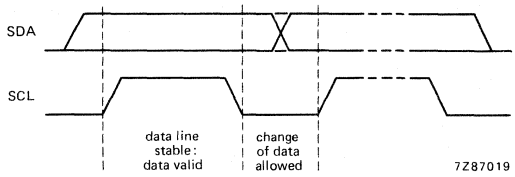


Fig. 3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

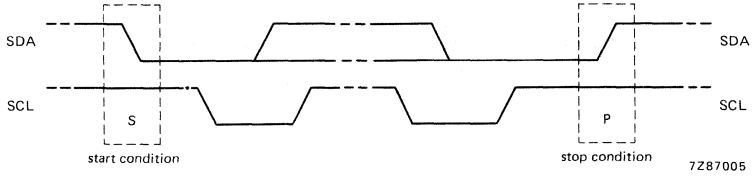


Fig. 4 Definition of start and stop conditions.

System configuration (see Fig. 5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

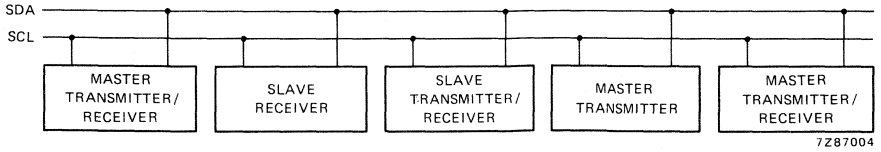


Fig. 5 System configuration.

CHARACTERISTICS OF THE I²C bus (continued)

Acknowledge (see Fig. 6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig. 13 and Fig. 14.)

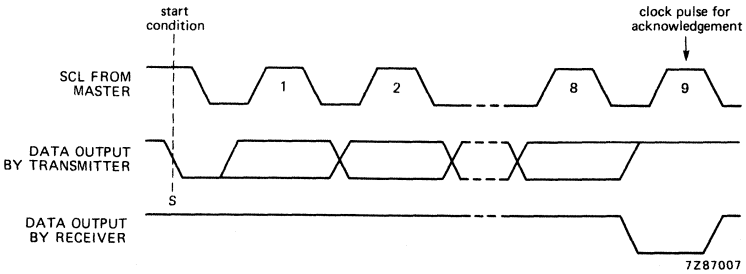


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8573 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

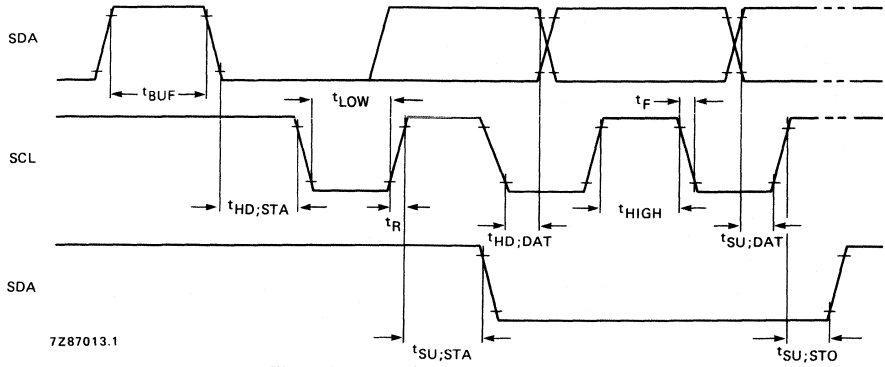


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}.

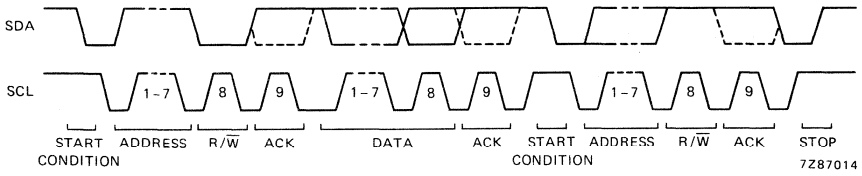


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

CHARACTERISTICS OF THE I²C BUS (continued)

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

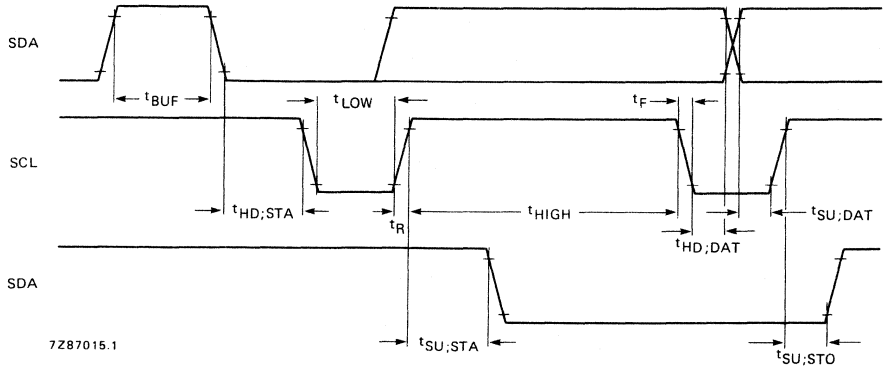


Fig. 9 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs*
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}, for definitions see high-speed mode.

* Only valid for repeated start code.

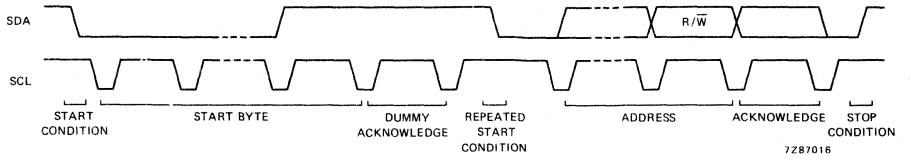


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig. 11.

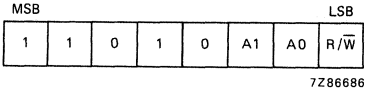


Fig. 11 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I²C bus configuration for different clock/calendar READ and WRITE cycles is shown in Fig. 12 and Fig. 13.

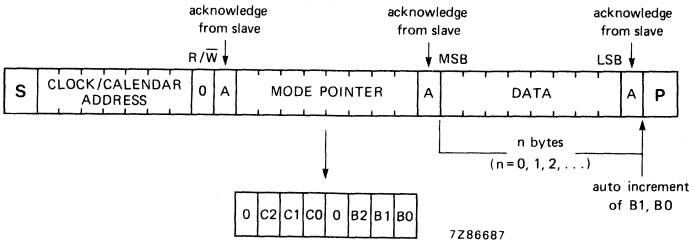


Fig. 12 Master transmitter transmits to clock/calendar slave receiver.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nibble is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

DEVELOPMENT SAMPLE DATA

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

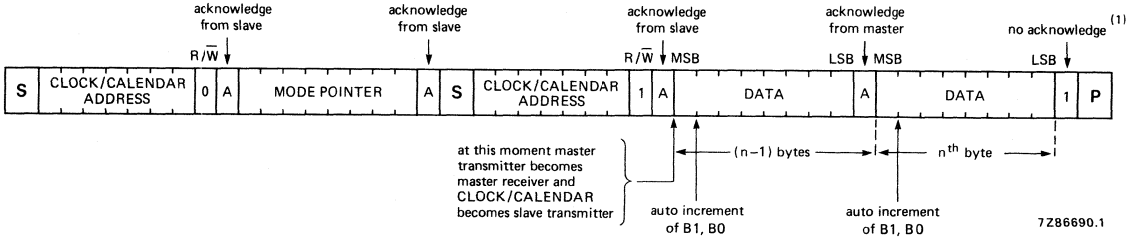
Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB				DATA			LSB	
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where "X" is the don't care bit and "D" is the data bit.

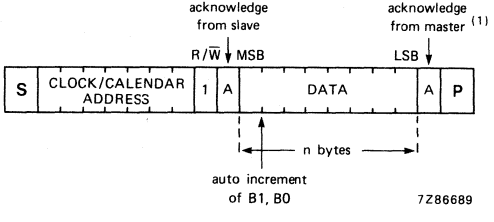
Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 13 Master transmitter reads clock/calendar after setting mode pointer.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 14 Master reads clock/calendar immediately after first byte.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER condition occurs.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

mode pointer								acknowledge on byte		
								address	mode pointer	data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where "X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	*	**	NODA	COMP	POWF	control/status flags

Where: "D" is the data bit.
* = minutes.
** = seconds.

DEVELOPMENT SAMPLE DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges	$V_{DD}-V_{SS1}$		−0,3 to + 8	V
	$V_{DD}-V_{SS2}$		−0,3 to + 8	V
Voltage on pins 4 and 5			V_{SS2}−0,8 to V_{DD} + 0,8	V*
Voltage on pins 6, 7, 13 and 14			V_{SS1}−0,6 to V_{DD} + 0,6	V
Voltage on any other pin			V_{SS2}−0,6 to V_{DD} + 0,6	V
Input current	I_I	max.	10	mA
Output current	I_O	max.	10	mA
Power dissipation per output	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	200	mW
Operating ambient temperature range	T_{amb}		−40 to + 85	°C
Storage temperature range	T_{stg}		−55 to + 125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* Impedance min. 500 Ω.

CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified. Typical values at T_{amb} = + 25 °C

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (I^2C interface)	$V_{DD}-V_{SS2}$	2,5	5	6,0	V
Supply voltage (clock)	$V_{DD}-V_{SS1}$	1,1	1,5	$(V_{DD}-V_{SS2})$	V
Supply current V_{SS1}					
at $V_{DD}-V_{SS1}$ = 1,5 V	$-I_{SS1}$	–	3	10	μA
at $V_{DD}-V_{SS1}$ = 5 V	$-I_{SS1}$	–	12	50	μA
Supply current V_{SS2}					
at $V_{DD}-V_{SS2}$ = 5 V (I_O = 0 mA on all outputs)	$-I_{SS2}$	–	–	50	μA
Inputs SCL, SDA, A0, A1, TEST					
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	–	V
Input voltage LOW	V_{IL}	–	–	0,3 x V_{DD}	V
Input leakage current					
at V_I = V_{SS2} to V_{DD}	$\pm I_I$	–	–	1	μA
Inputs EXTPF, PFIN					
Input voltage HIGH	$V_{IH}-V_{SS1}$	0,7 x $(V_{DD}-V_{SS1})$	–	–	V
Input voltage LOW	$V_{IL}-V_{SS1}$	0	–	0,3 x $(V_{DD}-V_{SS1})$	V
Input leakage current					
at V_I = V_{SS1} to V_{DD}	$\pm I_I$	–	–	1	μA
at T_{amb} = 25 °C; V_I = V_{SS1} to V_{DD}	$\pm I_I$	–	–	0,1	μA
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)					
Output voltage HIGH					
at $V_{DD}-V_{SS2}$ = 2,5 V; $-I_O$ = 0,1 mA	V_{OH}	V_{DD}−0,4	–	–	V
at $V_{DD}-V_{SS2}$ = 4 to 6 V; $-I_O$ = 0,5 mA	V_{OH}	V_{DD}−0,4	–	–	V
Output voltage LOW					
at $V_{DD}-V_{SS2}$ = 2,5 V; I_O = 0,3 mA	V_{OL}	–	–	0,4	V
at $V_{DD}-V_{SS2}$ = 4 to 6 V; I_O = 1,6 mA	V_{OL}	–	–	0,4	V

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Output SDA (N-channel open drain)					
Output "ON": I_O = 3 mA at $V_{DD}-V_{SS2}$ = 2,5 to 6 V	V_{OL}	–	–	0,4	V
Output "OFF" (leakage current) at $V_{DD}-V_{SS2}$ = 6 V; V_O = 6 V	I_O	–	–	1	μA
Internal threshold voltage					
Power failure detection	V_{TH1}	1	1,2	1,4	V
Power "ON" reset at $V_{SCL} = V_{SDA} = V_{DD}$	V_{TH2}	1,5	2,0	2,5	V
Rise and fall times of input signals					
Input EXTPF	t_r, t_f	–	–	1	μs
Input PFIN	t_r, t_f	–	–	∞	μs
Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels					
rise time	t_r	–	–	1	μs
fall time	t_f	–	–	0,3	μs
Frequency at SCL at $V_{DD}-V_{SS2}$ = 4 to 6 V					
Pulse width LOW (see Figs 7 and 9)	t_{LOW}	4,7	–	–	μs
Pulse width HIGH (see Figs 7 and 9)	t_{HIGH}	4	–	–	μs
Noise suppression time constant at SCL and SDA input	T_I	0,25	1	2,5	μs
Input capacitance (SCL, SDA)	C_I	–	–	7	pF
Oscillator					
Integrated oscillator capacitance	C_{out}	–	40	–	pF
Oscillator feedback resistance	R_f	–	3	–	MΩ
Oscillator stability for: $\Delta(V_{DD}-V_{SS1})$ = 100 mV at $V_{DD}-V_{SS1}$ = 1,55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-6}	–	–
Quartz crystal parameters					
Frequency = 32,768 kHz					
Series resistance	R_S	–	–	40	kΩ
Parallel capacitance	C_L	–	9	–	pF
Trimmer capacitance	C_T	5	–	25	pF

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

APPLICATION INFORMATION

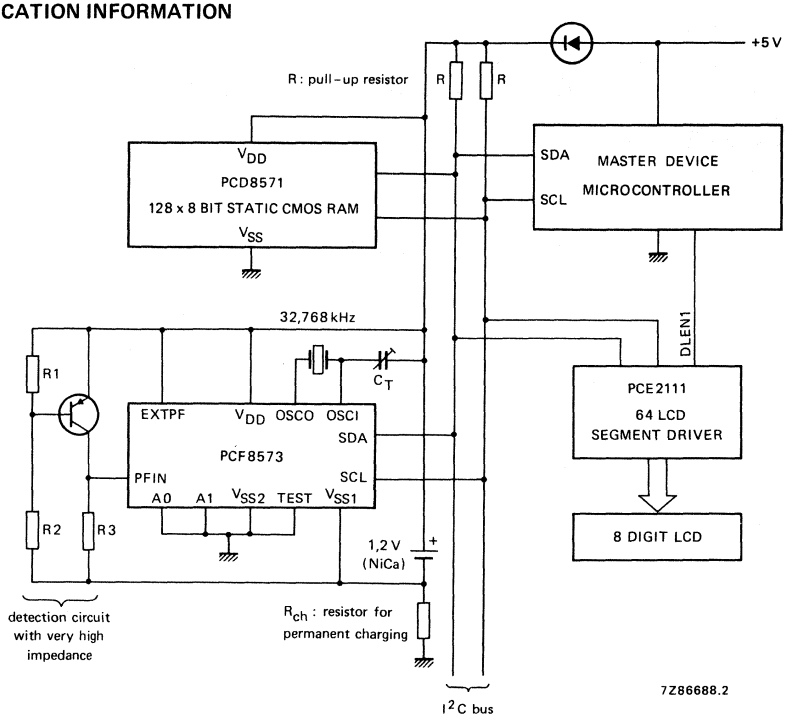


Fig. 15 Application example of the PCF8573 clock/calendar.

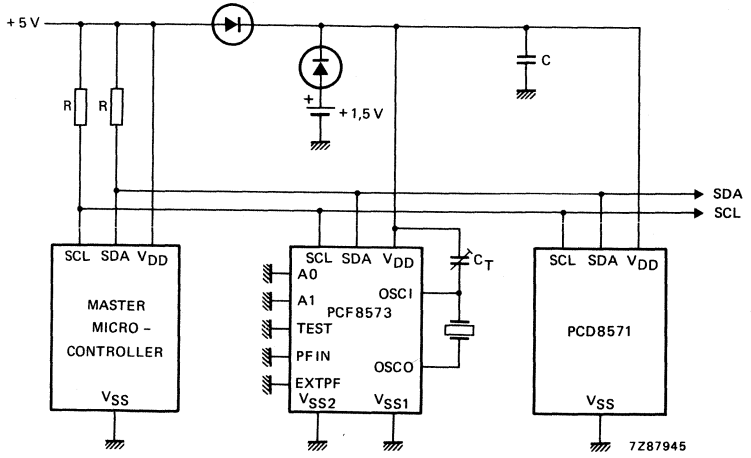


Fig. 16 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

REMOTE 8-BIT I/O FOR I²C BUS

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF8500 microcomputer families via the two-line serial bidirectional bus (I^2C).
It can also interface microcomputers without a serial interface to the I^2C bus (as a slave function only).
The device consists of an 8-bit quasi-bidirectional port and an I^2C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I^2C bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I^2C bus. This means that the PCF8574 can remain a simple slave device.

Features

- Operating supply voltage 2,5 V to 6 V
- Low stand-by current consumption max. 10 μA
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I^2C bus
- Peripheral for the MAB8400 and PCF8500 microcomputer families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 possible with mask option)

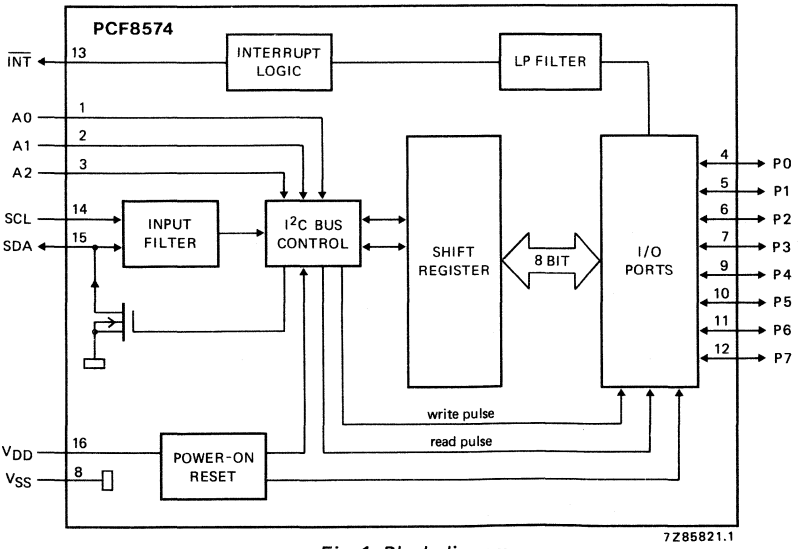


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8574P: 16-lead DIL; plastic (SOT-38).
PCF8574T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

PINNING

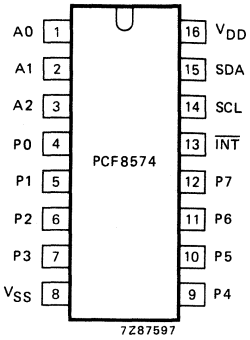


Fig. 2 Pinning diagram.

1 to 3	A0 to A2	address inputs
4 to 7 9 to 12	P0 to P3 P4 to P7	8-bit quasi-bidirectional I/O port
8	V_{SS}	negative supply
13	$\overline{INT}$	interrupt output
14	SCL	serial clock line
15	SDA	serial data line
16	V_{DD}	positive supply

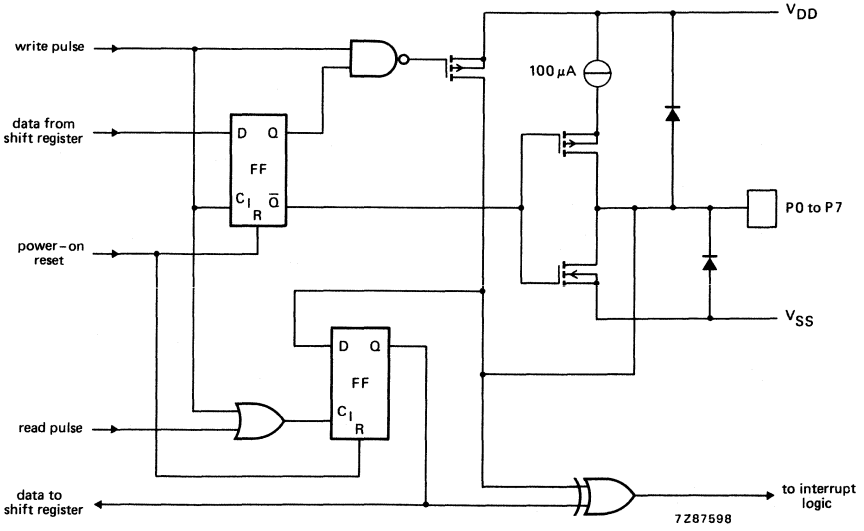


Fig. 3 Simplified schematic diagram of each port.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

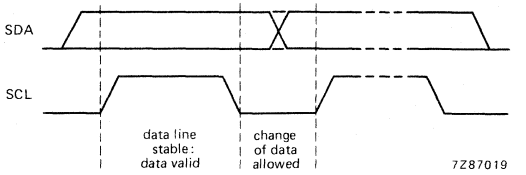


Fig. 4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

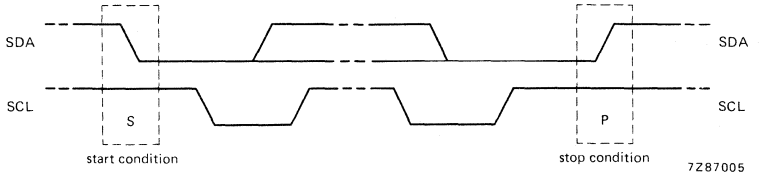


Fig. 5 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

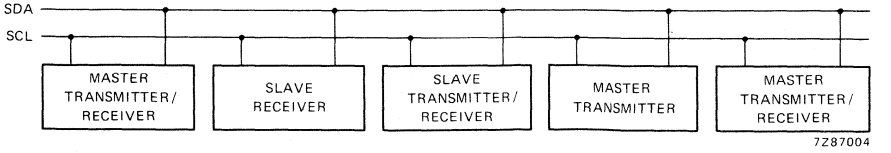


Fig. 6 System configuration.

CHARACTERISTICS OF THE I²C BUS (continued)

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

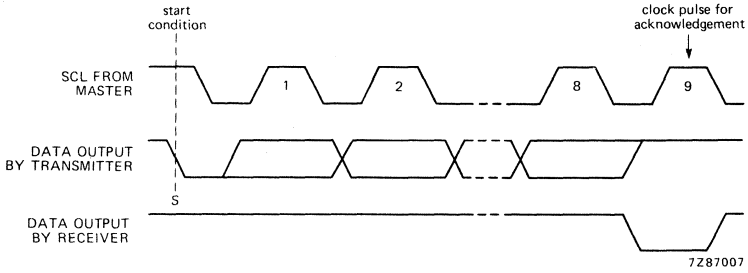


Fig. 7 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8574 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 8.

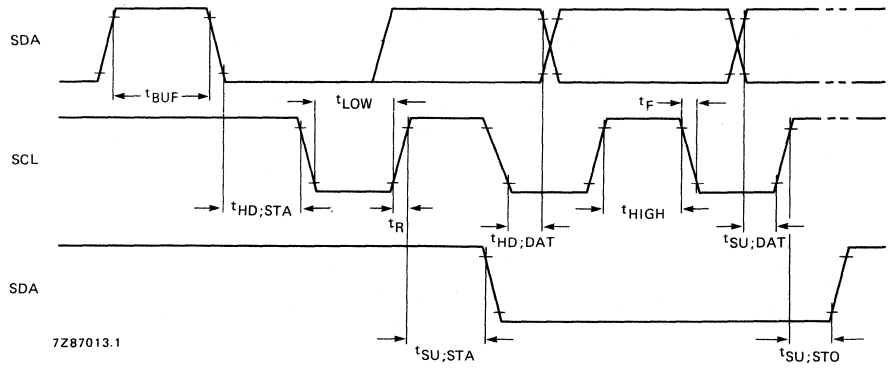


Fig. 8 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

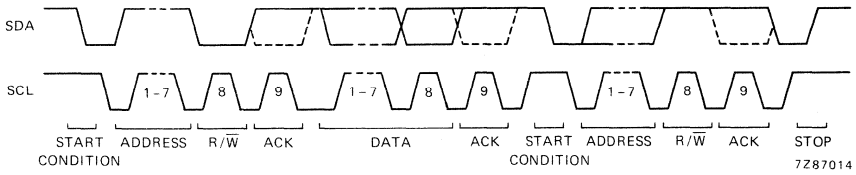


Fig. 9 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

CHARACTERISTICS OF THE I²C BUS (continued)

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 10.

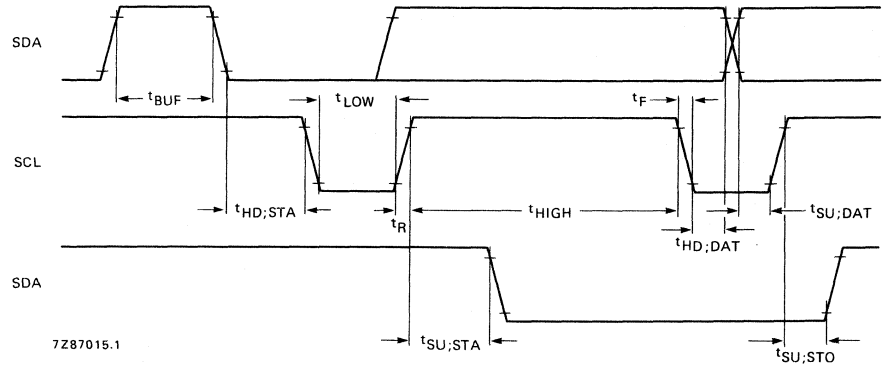


Fig. 10 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs*
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}, for definitions see high-speed mode.

* Only valid for repeated start code.

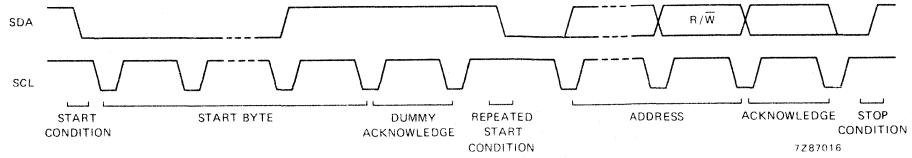


Fig. 11 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

FUNCTIONAL DESCRIPTION

Addressing (see Figs 12 and 13)

Each bit of the PCF8574 I/O port can be independently used as an input or an output. Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

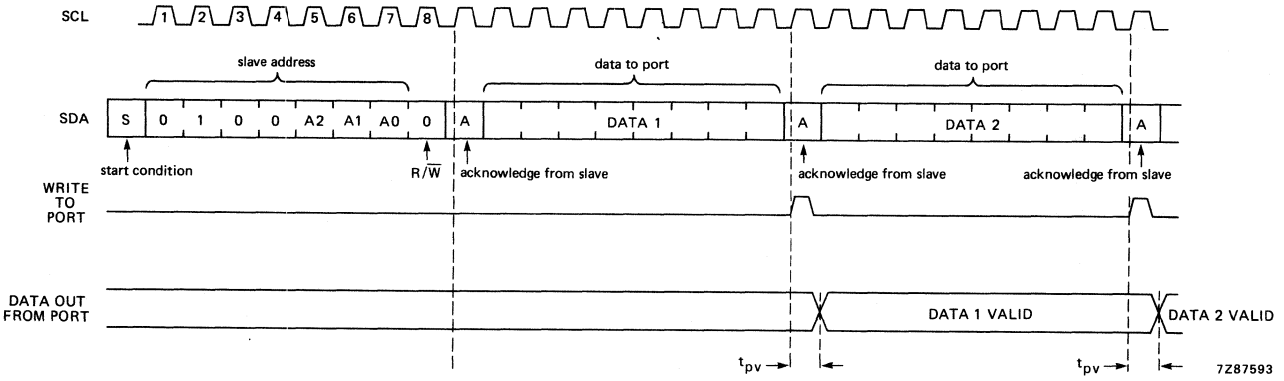


Fig. 12 WRITE mode (output port).

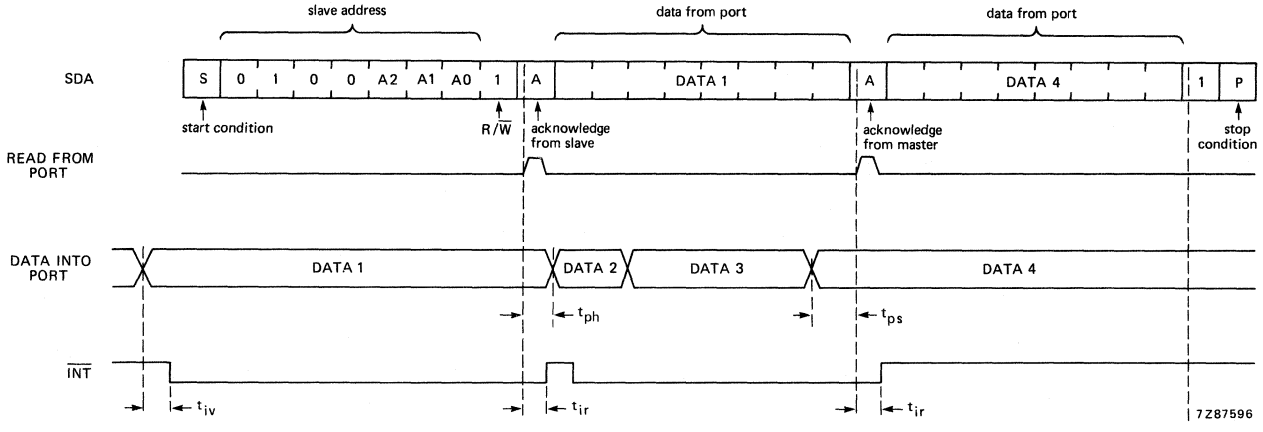


Fig. 13 READ mode (input port).

Note

A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Interrupt (see Figs 14 and 15)

The PCF8574 provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

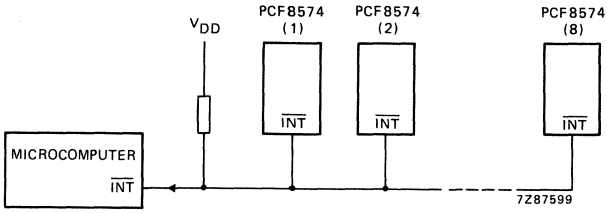


Fig. 14 Application of multiple PCF8574s with interrupt.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.
Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.
Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH to LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$.
Reading from or writing to another device does not affect the interrupt circuit.

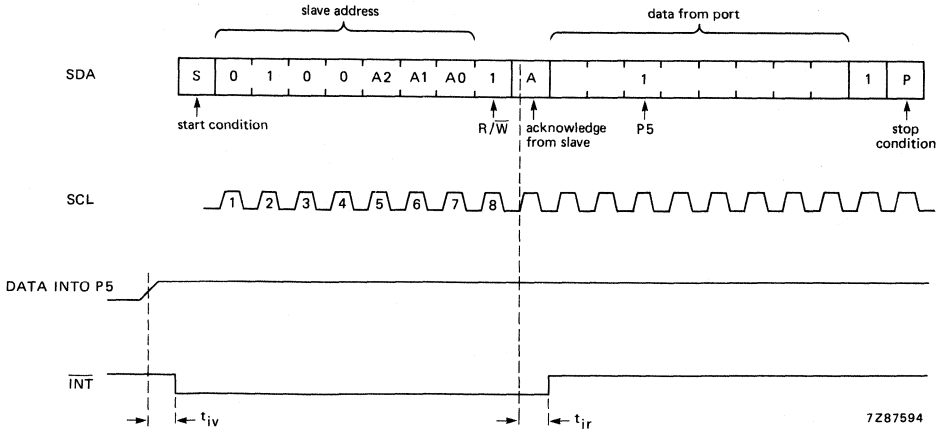


Fig. 15 Interrupt generated by a change of input to port P5.

FUNCTIONAL DESCRIPTION (continued)

Quasi-bidirectional I/O ports (see Fig. 16)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. The bit designated as an input must first be loaded with a logic 1. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output changes from LOW to HIGH, and are switched off by the negative edge of SCL. SCL should not remain HIGH when a short-circuit to V_{SS} is allowed (input mode).

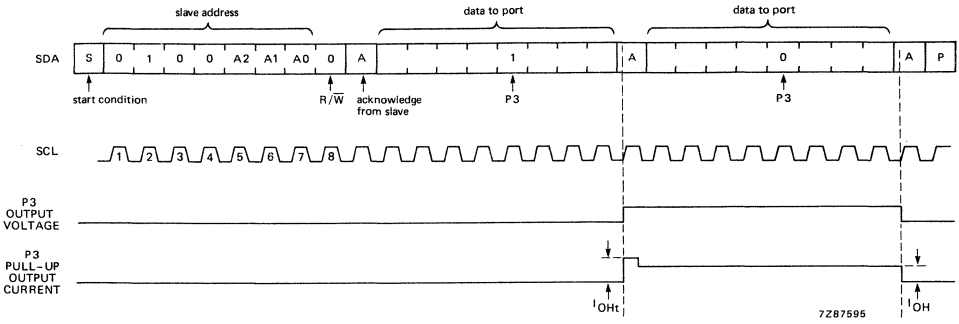


Fig. 16 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to + 7 V
Input voltage range (any pin)	V_I	V_{SS}	−0,5 to V_{DD} + 0,5 V
D.C. current into any input	$\pm I_I$	max.	20 mA
D.C. current into any output	$\pm I_O$	max.	25 mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; I_{SS}	max.	100 mA
Total power dissipation	P_{tot}	max.	400 mW
Power dissipation per output	P_o	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Operating ambient temperature range	T_{amb}		−40 to + 85 °C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current					
at V_{DD} = 6 V; no load, inputs at V_{DD}, V_{SS}					
operating; (SCL = 100 kHz)	I_{DD}	–	40	100	μA
standby	I_{DDO}	–	1,5	10	μA
Power-on reset voltage level (note 1)	V_{REF}	–	1,3	2,4	V
Input SCL; input/output SDA (pins 14; 15)					
Input voltage LOW	V_{IL}	−0,5 V	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD} + 0,5 V	V
Output current LOW					
at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Input/Output leakage current	$\|I_L\|$	–	–	100	nA
Clock frequency (see Fig. 8)	f_{SCL}	–	–	100	kHz
Tolerable spike width					
at SCL and SDA input	t_s	–	–	100	ns
Input capacitance (SCL, SDA)					
at V_I = V_{SS}	C_I	–	–	7	pF
I/O ports (pins 4 to 7; 9 to 12)					
Input voltage LOW	V_{IL}	−0,5 V	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD} + 0,5 V	V
Maximum allowed input current through protection diode					
at $V_I \geqslant V_{DD}$ or $\leqslant V_{SS}$	$\pm I_{IHL}$	–	–	400	μA
Output current LOW					
at V_{OL} = 1 V; V_{DD} = 5 V	I_{OL}	10	30	–	mA
Output current HIGH					
at V_{OH} = V_{SS} (current source only)	$-I_{OH}$	30	100	300	μA
Transient pull-up current HIGH during acknowledge (see Fig. 16)					
at V_{OH} = V_{SS}	$-I_{OHt}$	–	0,5	–	mA
Input/Output capacitance	$C_{I/O}$	–	–	10	pF
Port timing; $C_L \leqslant 100$ pF (see Figs 12 and 13)					
Output data valid	t_{pv}	–	–	4	μs
Input data set-up	t_{ps}	0	–	–	μs
Input data hold	t_{ph}	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
Interrupt $\overline{INT}$ (pin 13)					
Output current LOW at V_{OL} = 0,4 V	I_{OL}	1,6	–	–	mA
Output current HIGH at $V_{OH} = V_{DD}$	$\|I_{OH}\|$	–	–	100	nA
$\overline{INT}$ timing; $C_L \leqslant 100$ pF (see Fig. 13)					
Input data valid	t_{iv}	–	–	4	μs
Reset delay	t_{ir}	–	–	4	μs
Select inputs A0, A1, A2 (pins 1 to 3)					
Input voltage LOW	V_{IH}	−0,5 V	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD} + 0,5 V	V
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	100	nA

Note 1

The power-on reset circuit resets the I²C bus logic with $V_{DD} < V_{REF}$ and sets all ports to logic 1 (input mode with current source to V_{DD}).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO-56)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with Philips/Videlec chip-on-glass technology
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO-56; SOT-190).
PCF8576U: uncased chip in tray

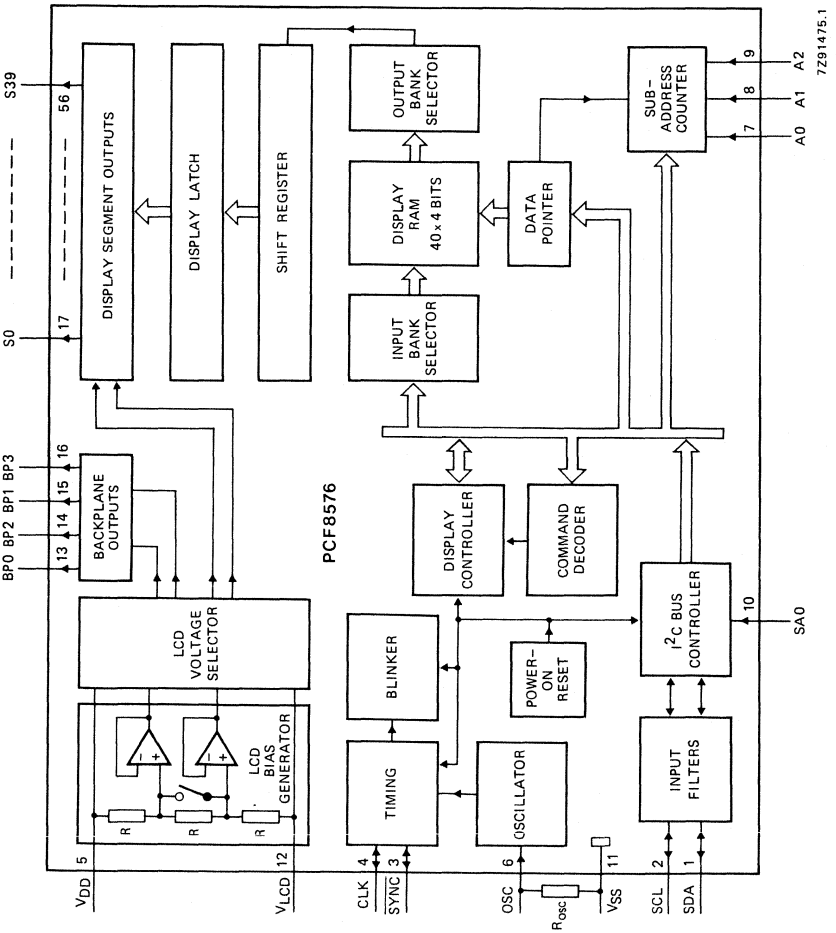


Fig. 1 Block diagram.

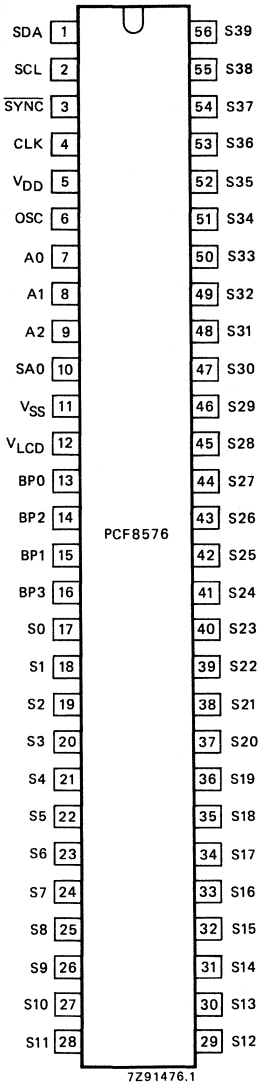


Fig. 2 Pinning diagram.

PINNING

1	SDA	I²C bus data input/output
2	SCL	I²C bus clock input/output
3	$\overline{\text{SYNC}}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I²C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I²C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17	S0	LCD segment outputs
to	to	
56	S39	

FUNCTIONAL DESCRIPTION

The PCF8576 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active back-plane outputs	no. of segmenets	7-segment numeric	14-segment alphanumeric	dot matrix
4	160	20 digits + 20 indicator symbols	10 characters + 20 indicator symbols	160 dots (4 x 40)
3	120	15 digits + 15 indicator symbols	8 characters + 8 indicator symbols	120 dots (3 x 40)
2	80	10 digits + 10 indicator symbols	5 characters + 10 indicator symbols	80 dots (2 x 40)
1	40	5 digits + 5 indicator symbols	2 characters + 12 indicator symbols	40 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor maintains the 2-line I²C bus communication channel with the PCF8576. A resistor connected between OSC (pin 6) and V_{SS} (pin 11) controls the device clock frequency. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

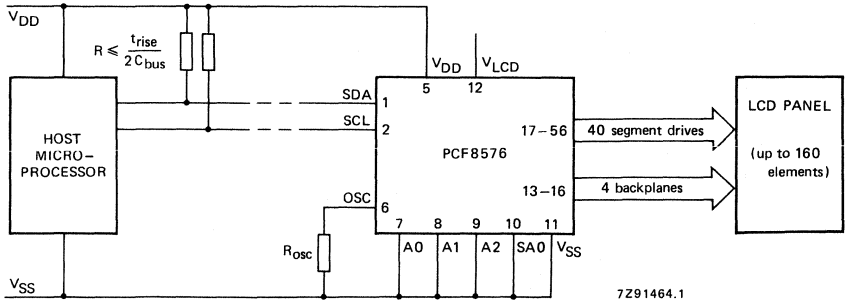


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8576 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I²C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I²C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{thLCD}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\,V_{thLCD}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1{,}732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1{,}528$ for 1 : 4 multiplex).
The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

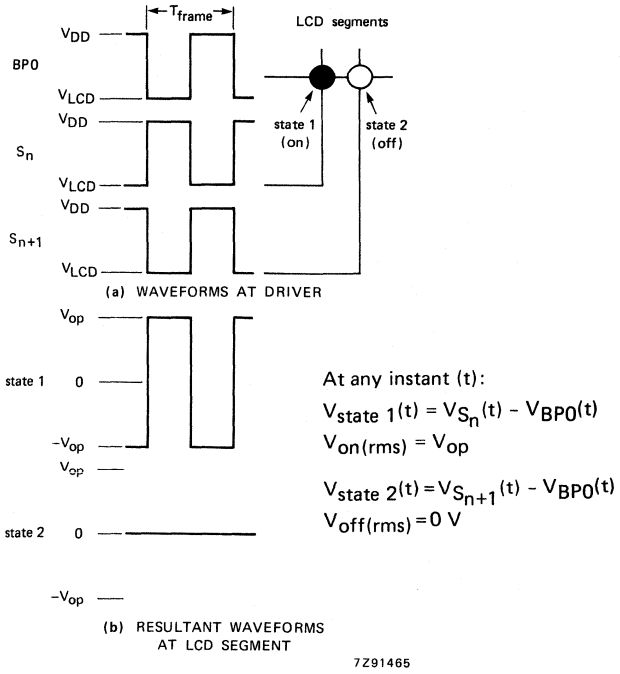
1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\,V_{off(rms)} = 2{,}449\,V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\;V_{off(rms)} = 2{,}309\,V_{off(rms)}$

These compare with $V_{op} = 3\,V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.



At any instant (t):

$V_{state\ 1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = V_{op}$

$V_{state\ 2}(t) = V_{S_{n+1}}(t) - V_{BP0}(t)$

$V_{off(rms)} = 0\ V$

Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8576 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

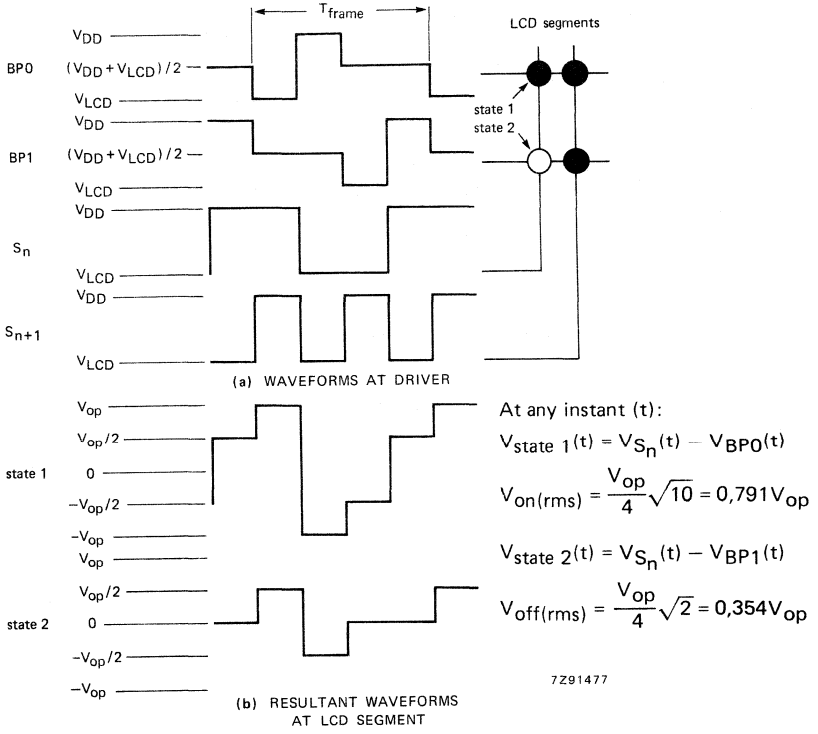


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

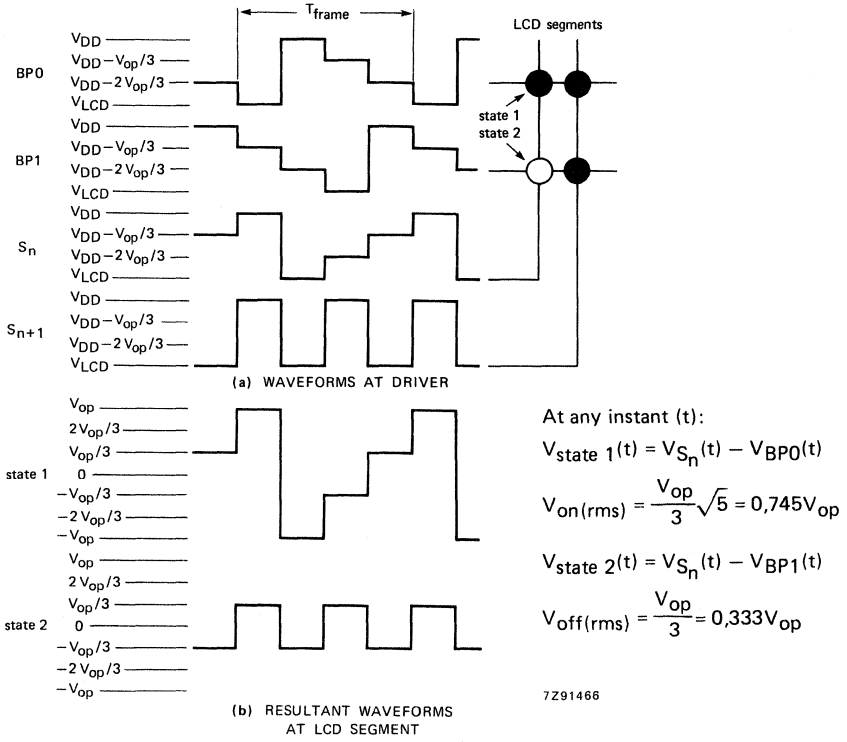


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive wavefront for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

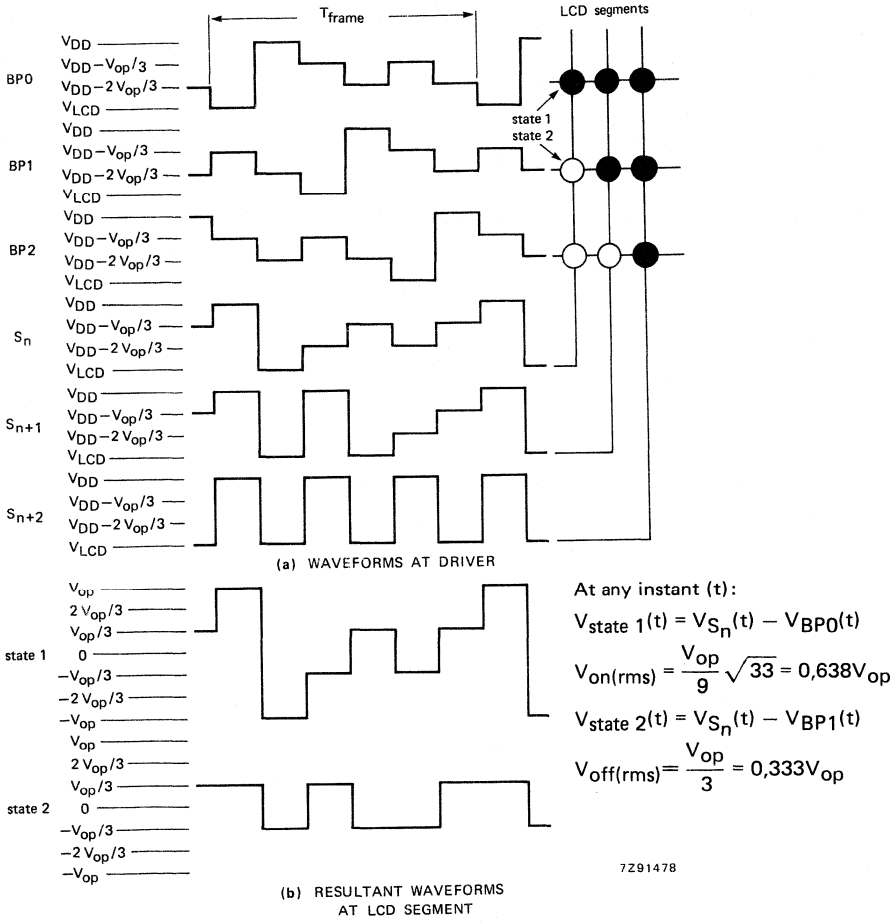


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

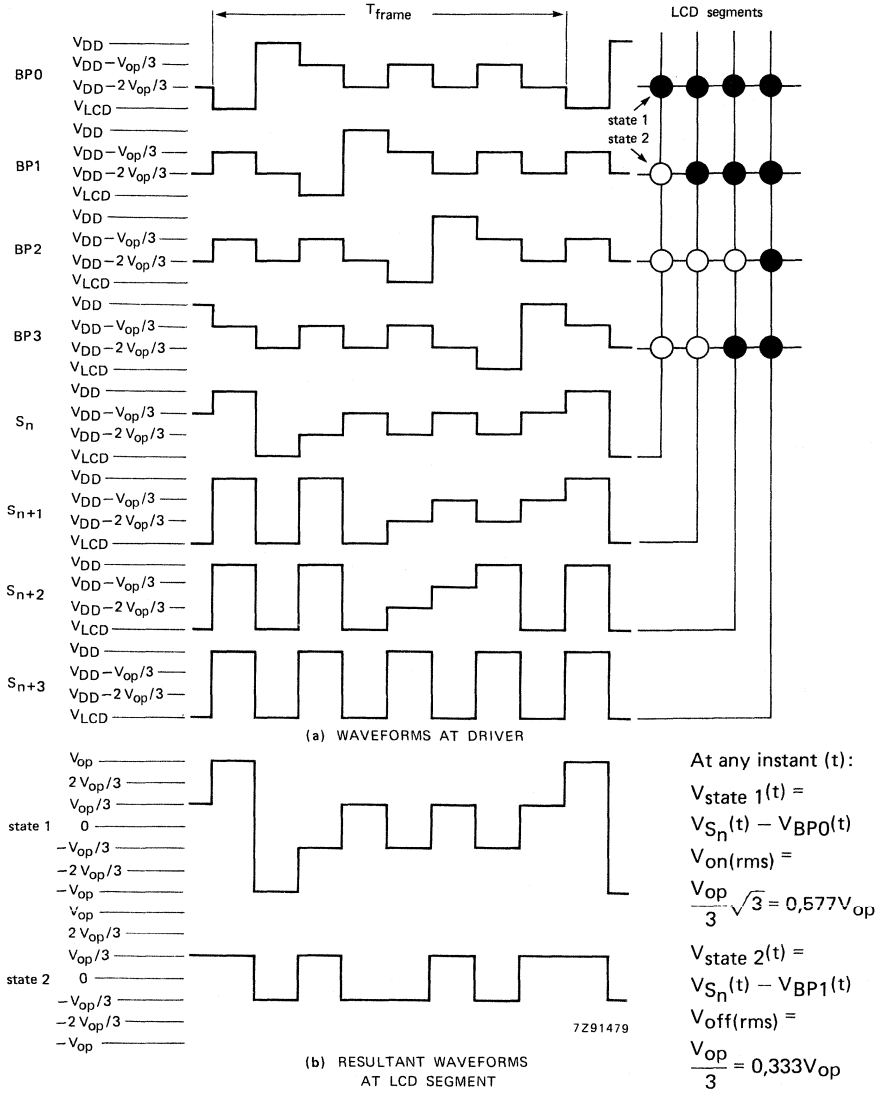


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

Internal clock

The internal logic and the LCD drive signals of the PCF8576 are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, frequency control is performed by a single resistor connected between OSC (pin 6) and V_{SS} (pin 11) as shown in Fig. 9. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8576s in the system.

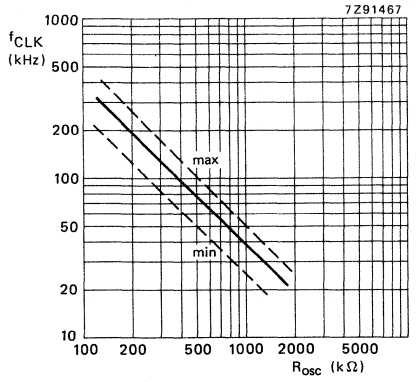


Fig. 9 Oscillator frequency as a function of R_{osc}: $f_{CLK} \approx (3{,}6 \times 10^7 / R_{osc})$ kHz·Ω.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I²C bus. To allow I²C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a d.c. state.

Timing

The timing of the PCF8576 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8576s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by the choice of value for R_{osc} when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8576 mode	recommended R_{osc} (kΩ)	f_{frame}	nominal f_{frame} (Hz)
normal mode	200	$f_{CLK}/2880$	64
power-saving mode	1200	$f_{CLK}/480$	64

Timing (continued)

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the normal mode, R_{OSC} = 200 kΩ will result in the nominal frame frequency. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six and for the same frame frequency R_{OSC} will be 1,2 MΩ. The reduced clock frequency and the increased value of R_{OSC} together contribute to a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 (pins 17 to 56) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 40 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (Fig. 10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

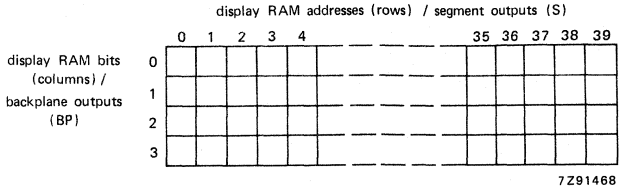


Fig. 10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8576 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 11; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

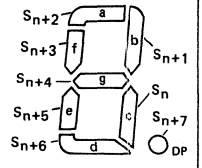
Data pointer

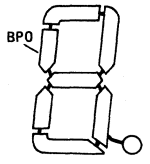
The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 11. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

static



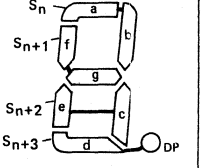


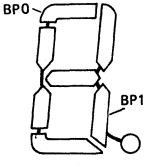
	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7
bit/ 0	c	b	a	f	g	e	d	DP
BP 1	x	x	x	x	x	x	x	x
2	x	x	x	x	x	x	x	x
3	x	x	x	x	x	x	x	x

msb lsb

c	b	a	f	g	e	d	DP

1 : 2 multiplex



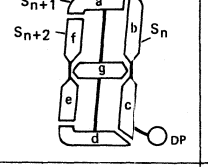


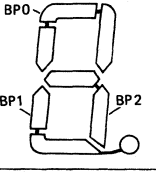
	n	n+1	n+2	n+3
bit/ 0	a	f	e	d
BP 1	b	g	c	DP
2	x	x	x	x
3	x	x	x	x

msb lsb

a	b	f	g	e	c	d	DP

1 : 3 multiplex



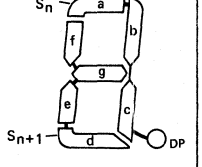


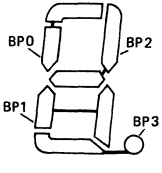
	n	n+1	n+2
bit/ 0	b	a	f
BP 1	DP	d	e
2	c	g	x
3	x	x	x

msb lsb

b	DP	c	a	d	g	f	e

1 : 4 multiplex





	n	n+1
bit/ 0	a	f
BP 1	c	e
2	b	g
3	DP	d

msb lsb

a	c	b	DP	f	e	g	d

Fig. 11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

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Subaddress counter (continued)

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8576 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8576 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Blinker (continued)

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

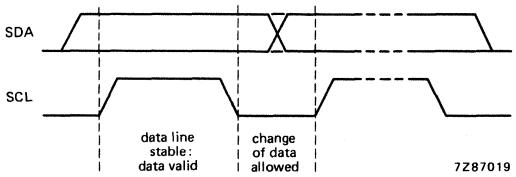


Fig. 12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

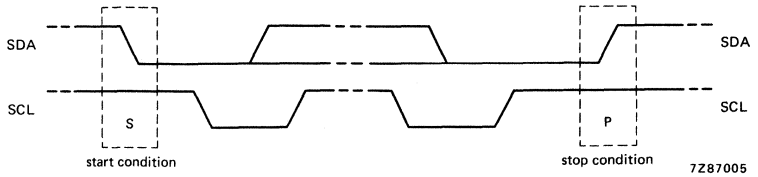


Fig. 13 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

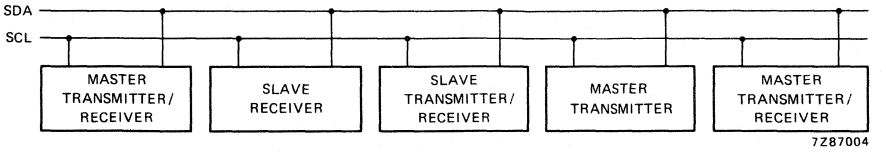


Fig. 14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

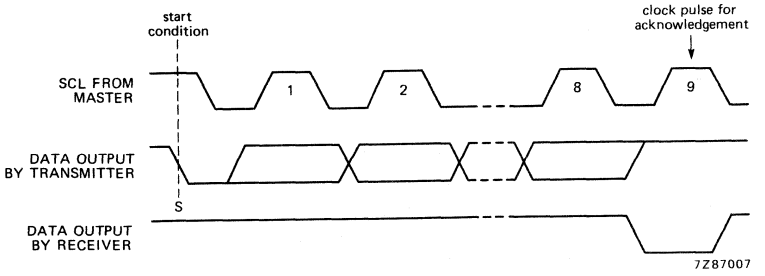


Fig. 15 Acknowledgement on the I^2C bus.

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

PCF8576 I²C bus controller

The PCF8576 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8576 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111000 and 0111001) are reserved for PCF8576. The least-significant bit of the slave address that a PCF8576 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8576 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8576s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 16. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8576 slave addresses available. All PCF8576s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8576s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8576 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8576. After the last display byte, the I²C bus master issues a stop condition (P).

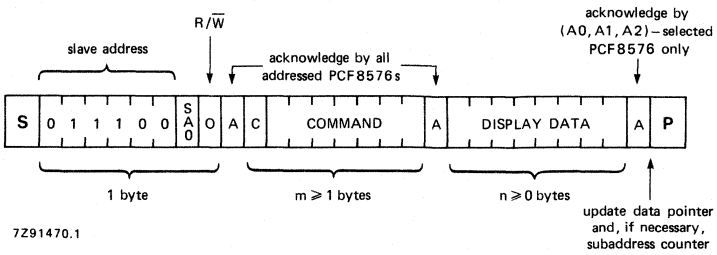


Fig. 16 I²C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I²C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 17). When this bit is set, it indicates that the next byte of the transfer will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

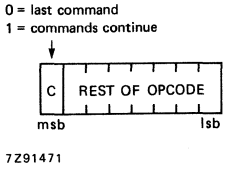


Fig. 17 General format of command byte.

The five commands available to the PCF8576 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8576 commands

command/opcode	options	description
MODE SET C 1 0 LP E B M1 M0	LCD drive mode: bits M1 M0 static (1 BP): 0 1 1 : 2 MUX (2 BP): 1 0 1 : 3 MUX (3 BP): 1 1 1 : 4 MUX (4 BP): 0 0 LCD bias: bit B 1/3 bias: 0 1/2 bias: 1 display status: bit E disabled (blank): 0 enabled: 1 mode: bit LP normal mode: 0 power-saving mode: 1	Defines LCD drive mode Defines LCD bias configuration Defines display status The possibility to disable the display allows implementation of blinking under external control Defines power dissipation mode
LOAD DATA POINTER C 0 P5 P4 P3 P2 P1 P0	bits P5 P4 P3 P2 P1 P0 6-bit binary value of 0 to 39	Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses
DEVICE SELECT C 1 1 0 0 A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7	Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

command/opcode	options	description
BANK SELECT C 1 1 1 1 0 I O	static / 1 : 2 MUX / bit I RAM bit 0 / RAM bits 0, 1 / 0 RAM bit 2 / RAM bits 2, 3 / 1 static / 1 : 2 MUX / bit O RAM bit 0 / RAM bits 0, 1 / 0 RAM bit 2 / RAM bits 2, 3 / 1	Defines input bank selection (storage of arriving display data) Defines output bank selection (retrieval of LCD display data) The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes
BLINK C 1 1 1 0 A BF1 BF0	blink frequency / bits BF1 BF0 off / 0 0 2 Hz / 0 1 1 Hz / 1 0 0,5 Hz / 1 1 blink mode / bit A normal blinking / 0 alternation blinking / 1	Defines the blinking frequency Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8576s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8576s. When cascaded, several PCF8576s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576s of the cascade contribute additional segment outputs but their backplane outputs are left open (Fig. 18).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8576s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576s with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8576 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8576 to assert $\overline{SYNC}$. The timing relationships between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576 are shown in Fig. 19.

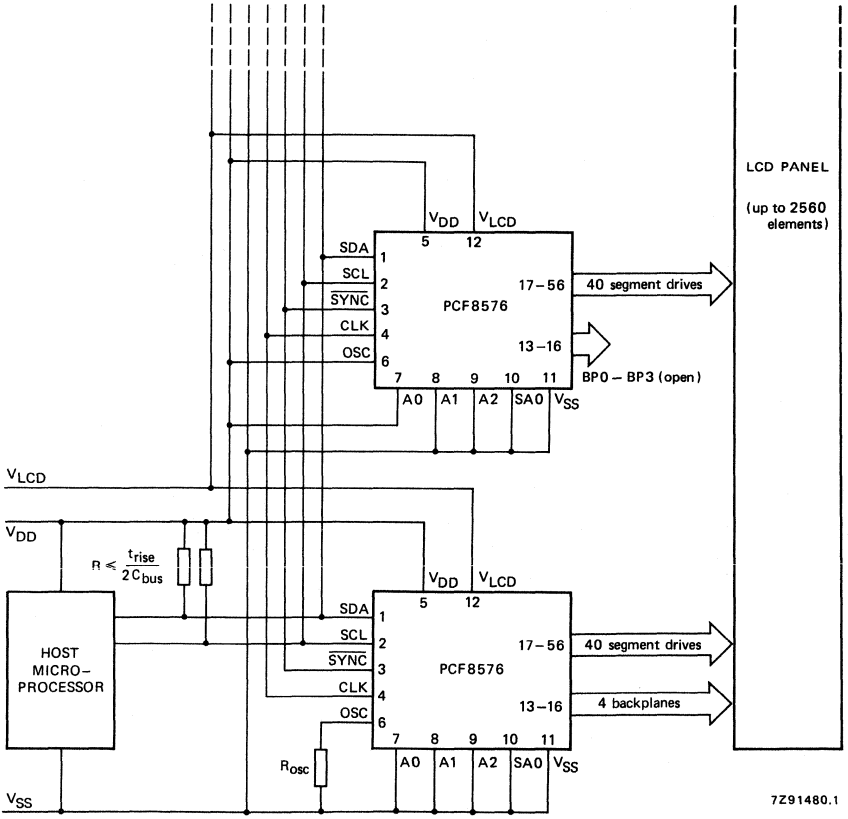


Fig. 18 Cascaded PCF8576 configuration.

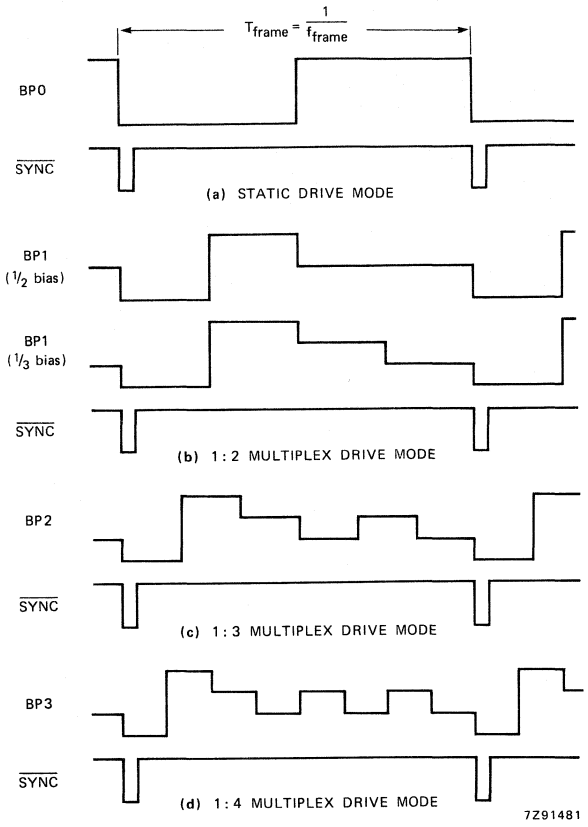


Fig. 19 Synchronization of the cascade for the various PCF8576 drive modes.

For single plane wiring of packaged PCF8576s and chip-on-glass cascading, see application information.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to + 11 V
LCD supply voltage range	V_{LCD}		V_{DD}−11 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I	V_{SS}	−0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S39; BP0 to BP3)	V_O	V_{LCD}	−0,5 to V_{DD} + 0,5 V
D.C. input current	$\pm I_I$	max.	20 mA
D.C. output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

D.C. CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2 to 9 V; V_{LCD} = V_{DD}−2 to V_{DD}−9 V;
T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2	–	9	V
LCD supply voltage (note 1)	V_{LCD}	V_{DD}−9	–	V_{DD}−2	V
Operating supply current at f_{CLK} = 200 kHz (note 2)	I_{DD}	–	–	tbf	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz (note 2)	I_{LP}	–	–	tbf	μA
LCD supply current at f_{CLK} = 200 kHz (note 2)	I_{LCD}	–	–	tbf	μA
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD}−0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	−1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0; A0 to A2; CLK; SCL; SDA) at V_I = V_{SS} or V_{DD}	$\pm I_{L1}$	–	–	1	μA

parameter	symbol	min.	typ.	max.	unit
Leakage current (OSC) at $V_I = V_{DD}$	$\pm I_{L2}$	–	–	1	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	30	60	100	kΩ
Power-on reset level (note 3)	V_{REF}	0,8	1,2	1,6	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 4)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S39) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}-5$ V (note 5)	R_{BP}	–	–	5	kΩ
Output impedance (S0 to S39) at $V_{LCD} = V_{DD}-5$ V (note 5)	R_S	–	–	7,0	kΩ

A.C. CHARACTERISTICS (note 6)

V_{SS} = 0 V; V_{DD} = 2 to 9 V; $V_{LCD} = V_{DD}-2$ to $V_{DD}-9$ V;
$T_{amb} = -40$ to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V; R_{osc} = 200 kΩ (note 7)	f_{CLK}	125	185	288	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V; R_{osc} = 1,2 MΩ	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	200	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at $V_{LCD} = V_{DD}-5$ V	t_{PLCD}	–	–	30	μs

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
I²C bus high-speed mode					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_R	–	–	1	μs
Fall time	t_F	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs
I²C bus low-speed mode					
Bus free time	t_{BUF}	105	–	–	μs
Start condition hold time	$t_{HD;STA}$	365	–	–	μs
SCL LOW time	t_{LOW}	105	–	155	μs
SCL HIGH time	t_{HIGH}	365	–	415	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	105	–	155	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_R	–	–	1	μs
Fall time	t_F	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	105	–	155	μs

Notes to characteristics

1. $V_{LCD} < V_{DD}-3$ V for 1/3 bias.
2. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty cycle; I²C bus inactive.
3. Resets all logic when $V_{DD} < V_{REF}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.
6. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
7. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

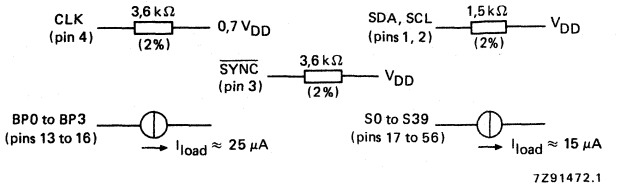


Fig. 20 Test loads.

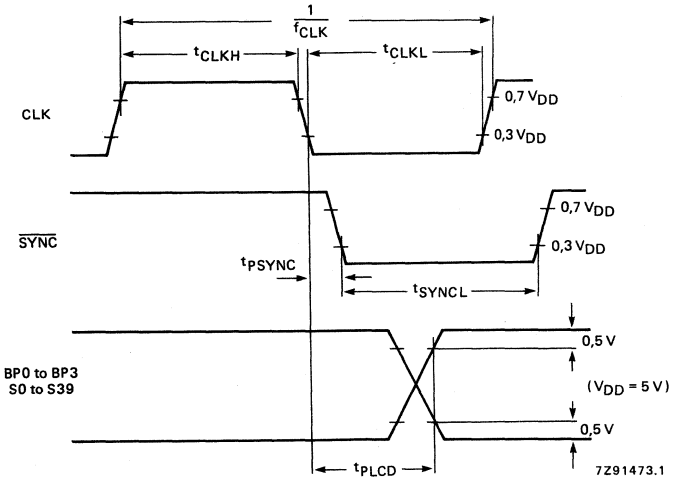


Fig. 21 Driver timing waveforms.

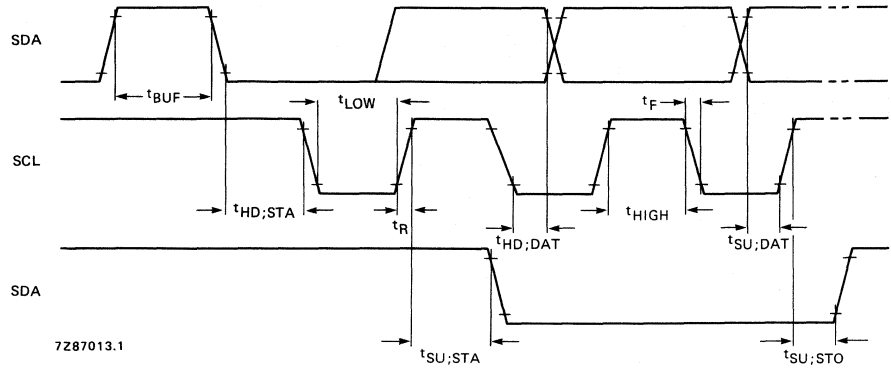


Fig. 22 I²C bus high-speed mode timing waveforms.

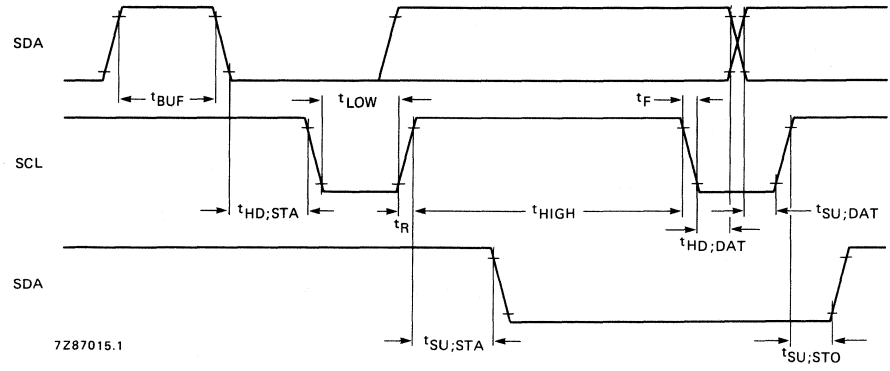


Fig. 23 I²C bus low-speed mode timing waveforms.

APPLICATION INFORMATION

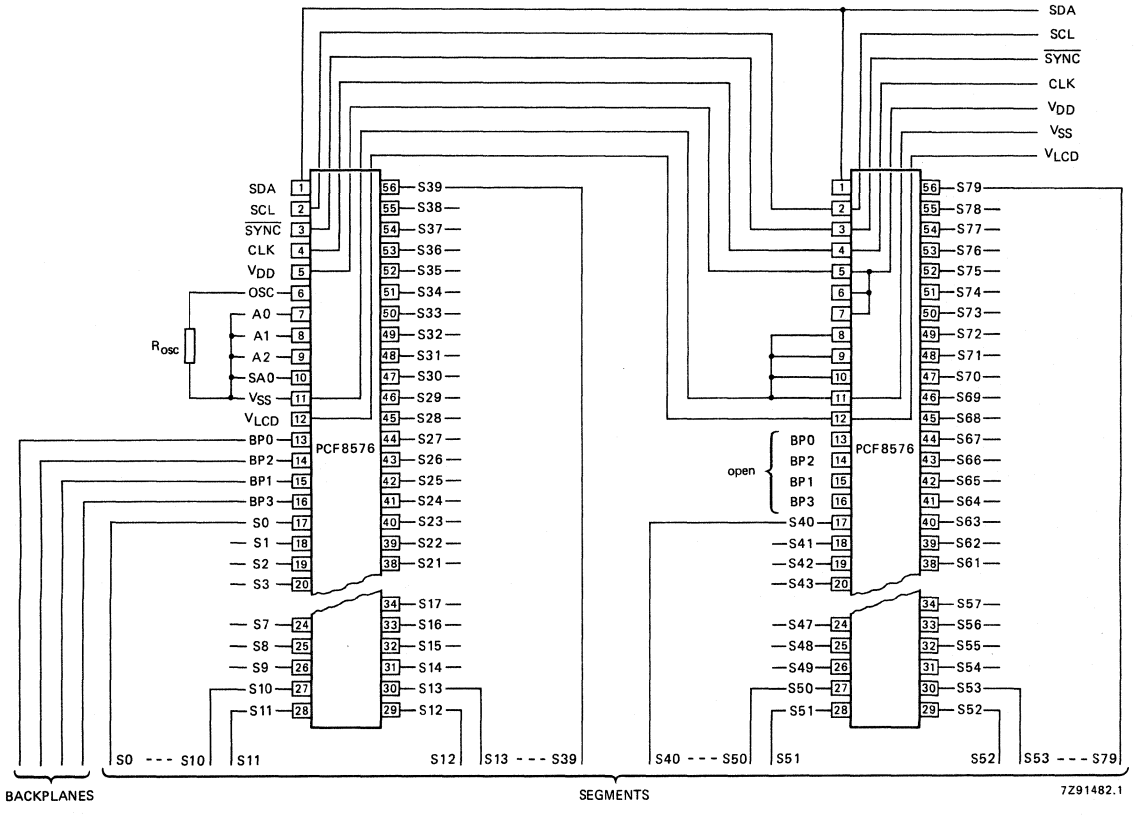


Fig. 24 Single plane wiring of packaged PCF8576s.

APPLICATION INFORMATION (continued)

Chip-on-glass cascadability in single plane

In chip-on-glass technology, where driver devices are bonded directly onto the glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576 bonding pad layout (Fig. 25). Pads needing bus interconnection between all PCF8576s of the cascade are V_{DD}, V_{SS}, CLK, SCL, SDA and $\overline{SYNC}$. These lines may be led to the corresponding pads of the next PCF8576 through the wide opening between the V_{LCD} pad and the backplane output pads. The only bussed line that does not require a second opening to lead through to the next PCF8576 is V_{LCD}, being the cascade centre. The placing of V_{LCD} adjacent to V_{SS} allows the two supplies to be tied together.

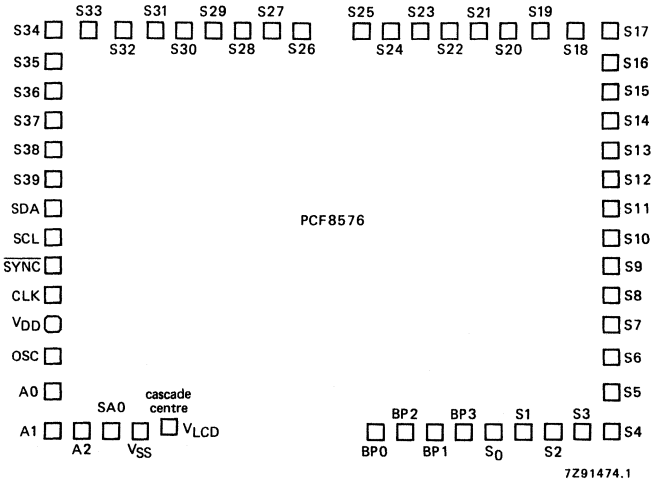


Fig. 25 PCF8576 bonding pad layout.

Fig. 26 shows the connection diagram for a cascaded PCF8576 application with single plane wiring. Note the use of the open space between the V_{LCD} pad and the backplane output pads to route V_{DD}, V_{SS}, CLK, SCL, SDA and $\overline{SYNC}$. The external connections may be made to either end of the cascade, wherever most convenient for the connector.

When an external clocking source is to be used, OSC of all devices should be tied to V_{DD}. The pads OSC, A0, A1, A2 and SA0 have been placed between V_{SS} and V_{DD} to facilitate wiring of oscillator, hardware subaddress and slave address.

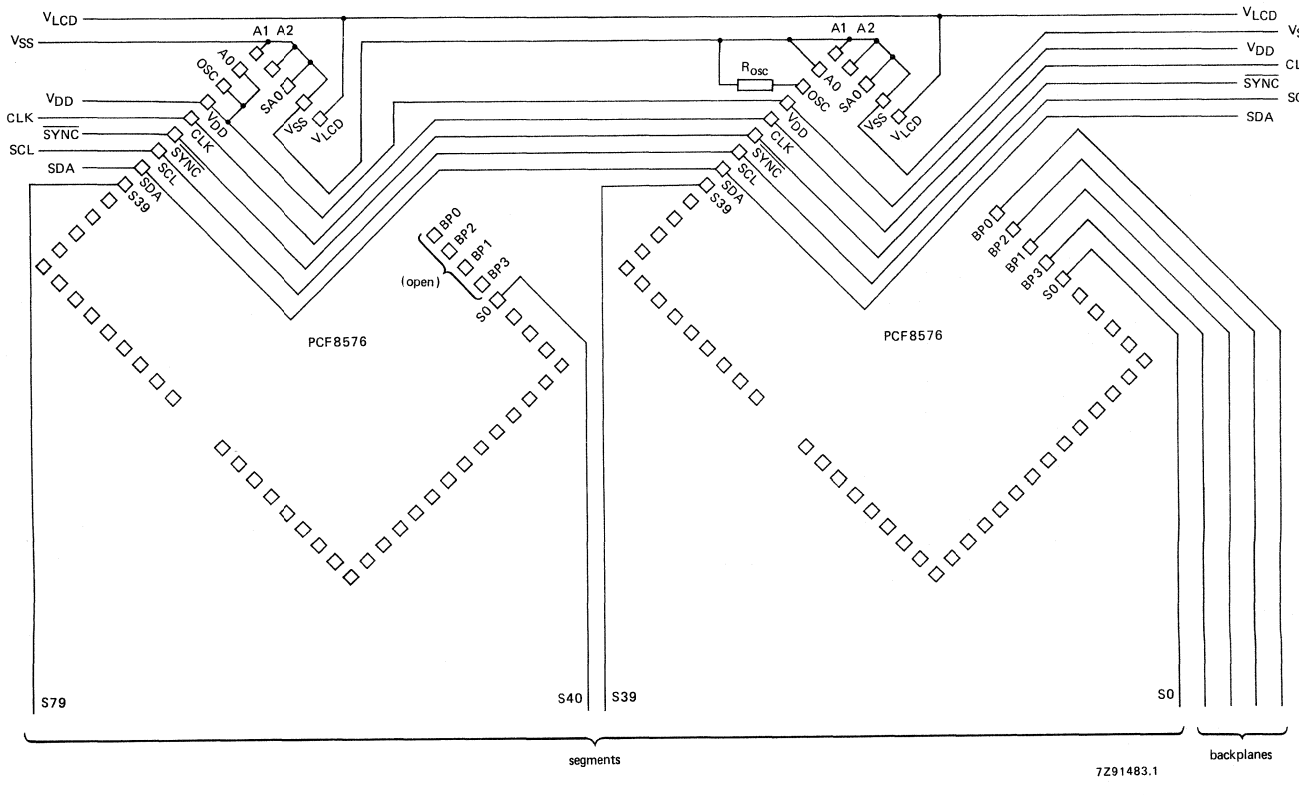


Fig. 26 Chip-on-glass application; cascaded PCF8576s with single-plane wiring (viewed from back of chip).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Videlec is a joint venture of BBC Brown Boveri and Philips specializing in liquid crystal display technology to meet the requirements of original equipment manufacturers.

Videlec AG
Hardstrasse 5
Lenzburg CH5600
Switzerland.

LCD DIRECT/DUPLEX DRIVER WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2,5 to 9 V
- Low power consumption
- I²C bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device sub-address boundaries
- Display memory switching in direct drive mode
- May be used for I²C bus output expander
- System expansion up to 256 segments
- Power-on-reset sets all segments off (to blank)

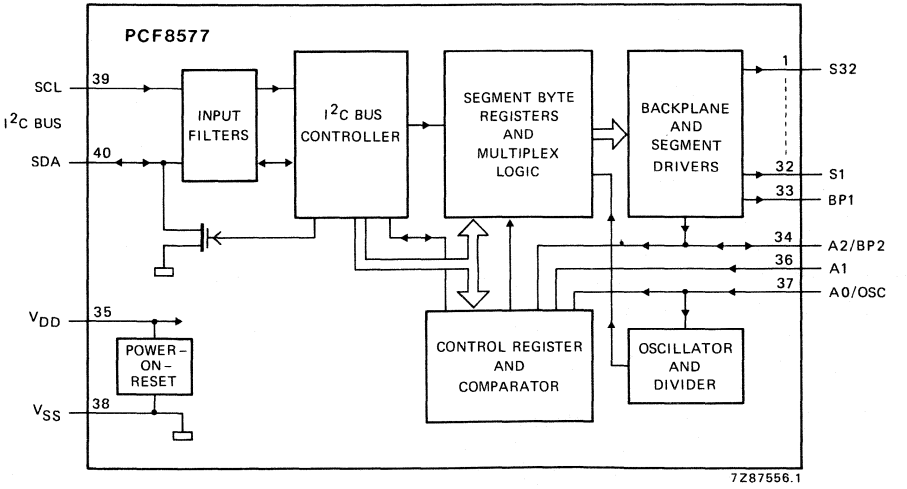


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8577P: 40-lead DIL; plastic (SOT-129).
PCF8577T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

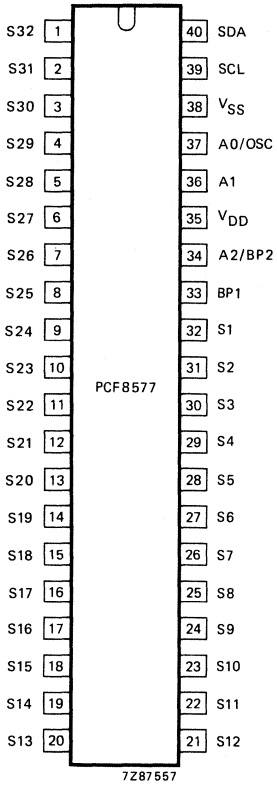


Fig. 2 Pinning diagram.

PINNING

Supply

35	V_{DD}	positive supply
38	V_{SS}	negative supply

I^2C bus

40	SDA	I^2C bus data line
39	SCL	I^2C bus clock line

Inputs

36	A1	hardware address line
37	A0/OSC	hardware address line/oscillator pin

Outputs

1 – 32	S1 – S32	segment outputs

Input – Output

34	A2/BP2	harware address line/cascade sync input/backplane output
33	BP1	cascade sync input/backplane output

FUNCTIONAL DESCRIPTION

Hardware sub-address A0, A1, A2

The hardware sub-address lines A0, A1, A2 are used to program the device sub-address for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

A0/OSC Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.

A1 Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.

A2/BP2 In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.

In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

Oscillator A0/OSC

The PCF8577 has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator. In an expanded system containing more than one PCF8577 the backplane signals are usually common to all devices and only one oscillator is needed. The devices which are not used for the oscillator are put into the expansion mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the expansion mode each PCF8577 is synchronized from the backplane signal(s).

User-accessible registers

There are nine user-accesible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even numbered segment byte registers is called BANK A. Odd numbered segment byte registers are called BANK B.

All PCF8577 have the same slave address (see Fig. 14). All devices load the second byte into the control register and each device maintains an identical copy of the control byte in the control register al all times (see I²C bus protocol Fig. 15).

The control register is shown in more detail in Fig. 3. The least-significant bits select which device and which segment byte register are loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).

The upper three bits of the SBV (V5 to V3) are compared with the hardware sub-address input signals A2, A1 and A0. If they are the same then the device is enabled for loading, if not the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

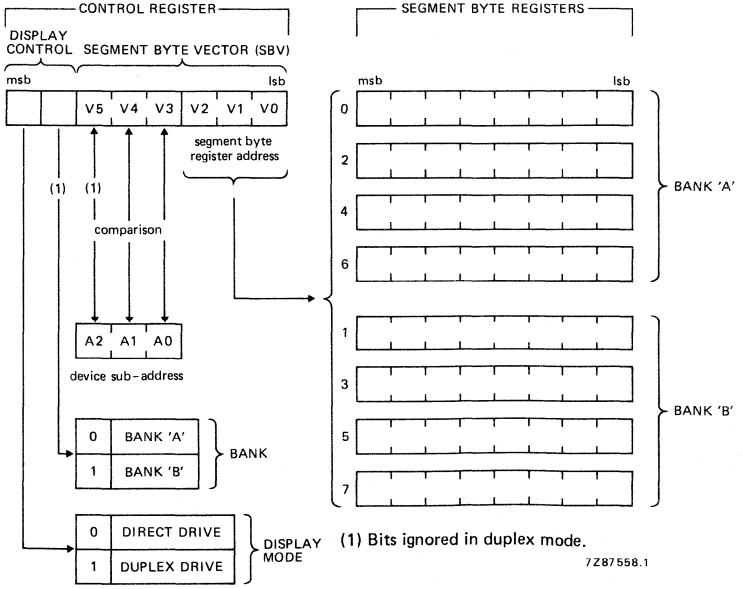


Fig. 3 PCF8577 register organization.

FUNCTIONAL DESCRIPTION (continued)

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct or duplex drive displays. The BANK bit allows the user to display BANK A or BANK B.

Auto-incremented loading

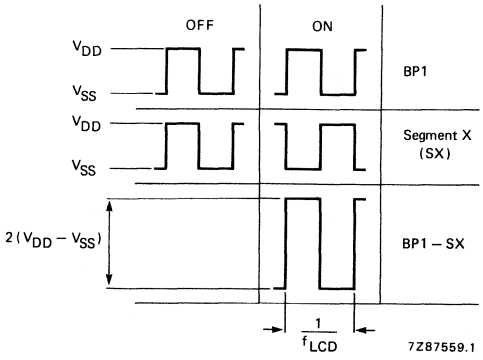
After each segment byte is loaded the SBV is incremented automatically, thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers, auto-incremented loading may proceed across device boundaries provided that the hardware sub-addresses are arranged contiguously.

Direct drive mode

The PCF8577 is set to the direct drive mode by loading the MODE control bit with logic 0. In this mode only four bytes are needed to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A); setting the BANK bit to logic 1 selects odd bytes (BANK B).

In the direct drive mode the SBV is auto-incremented by two after the loading of each segment byte register. This means that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded irrespective of which bank is being displayed. Direct drive output waveforms are shown in Fig. 4.



$V_{ON} = V_{DD} - V_{SS}$

$V_{OFF} = 0$

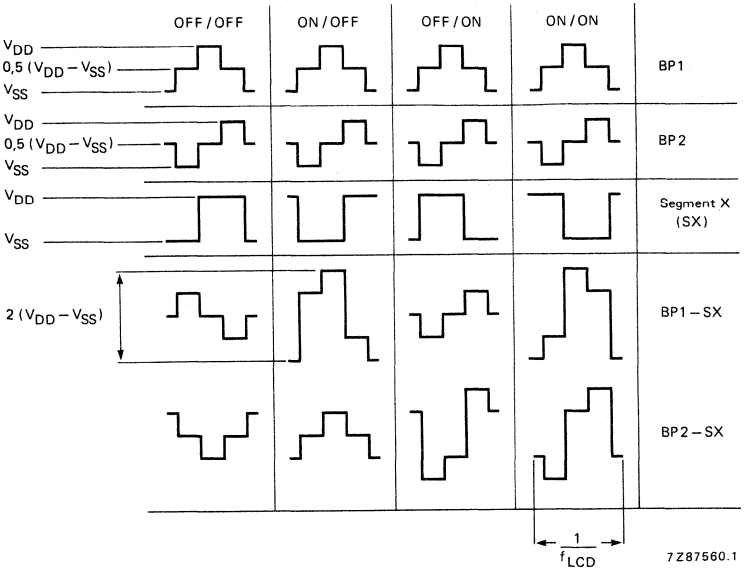
Fig. 4 Direct drive mode display output waveforms.

Duplex mode

The PCF8577 is set to the duplex mode by loading the MODE bit with logic 1. In this mode a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore A2 and its equivalent SBV bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are needed to store data for the 32 segment drivers and the BANK bit is ignored.

Duplex mode output waveforms are shown in Fig. 5.



$V_{ON} = 0{,}79\ (V_{DD} - V_{SS})$

$V_{OFF} = 0{,}35\ (V_{DD} - V_{SS})$

$\frac{V_{ON}}{V_{OFF}} = 2{,}26$

Fig. 5 Duplex mode display output waveforms.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

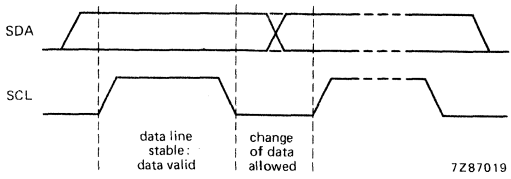


Fig. 6 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

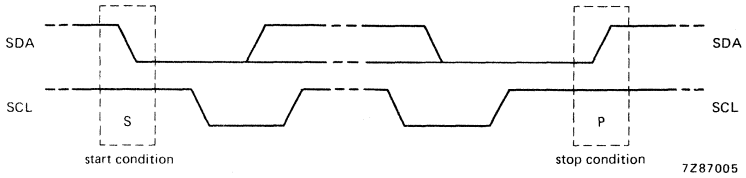


Fig. 7 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

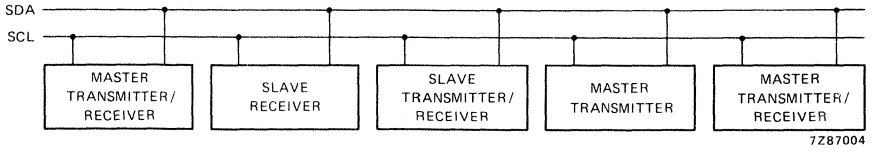


Fig. 8 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

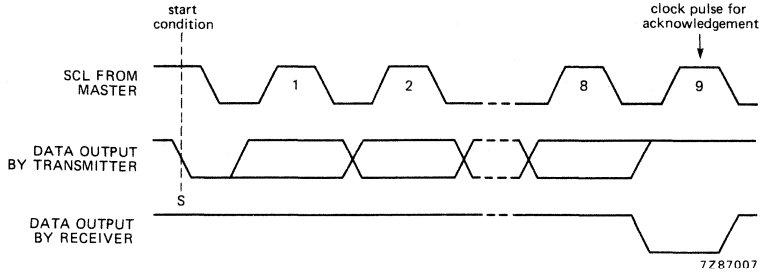


Fig. 9 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8577 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

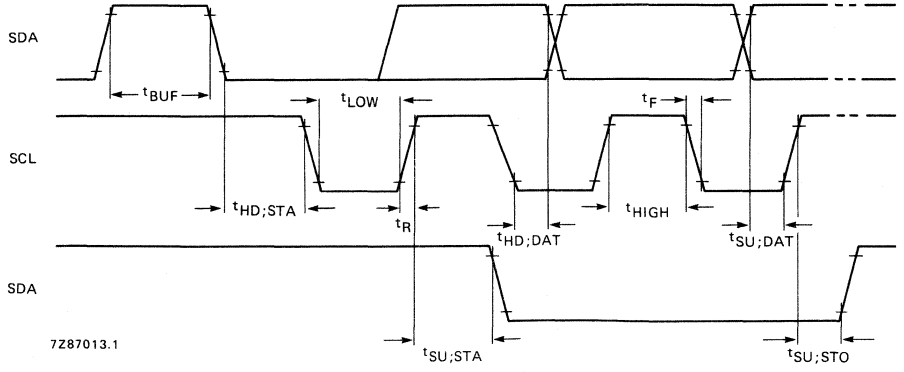


Fig. 10 Timing of the high-speed mode.

CHARACTERISTICS OF THE I²C BUS (continued)

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values referred to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

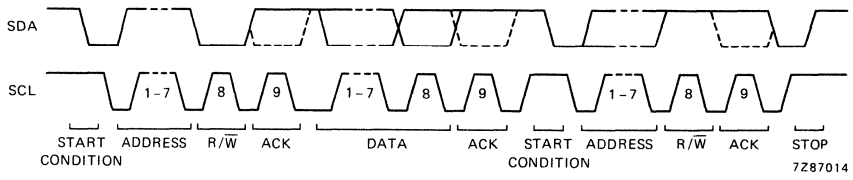


Fig. 11 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 12.

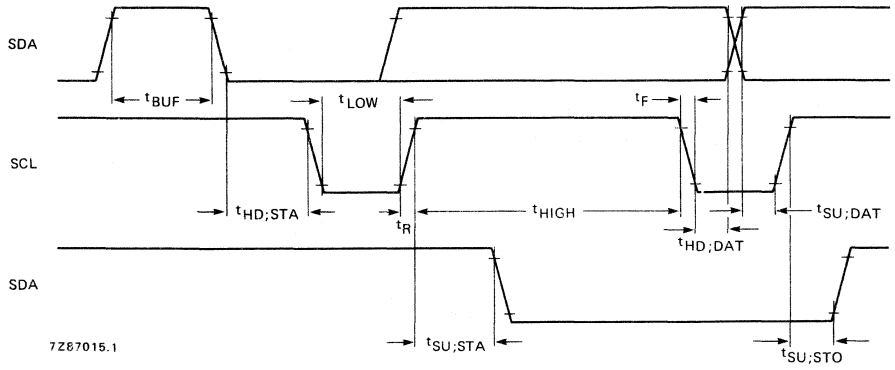


Fig. 12 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs*
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

Note

All the timing values referred to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}, for definitions see high-speed mode.

* Only valid for repeated start code.

CHARACTERISTICS OF THE I²C BUS (continued)

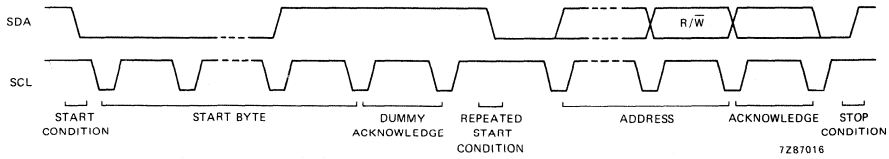


Fig. 13 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The slave address for PCF8577 is shown in Fig. 14.

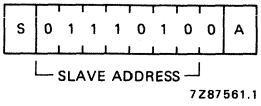


Fig. 14 PCF8577 slave address.

I²C bus protocol

The PCF8577 I²C bus protocol is shown in Fig. 15.

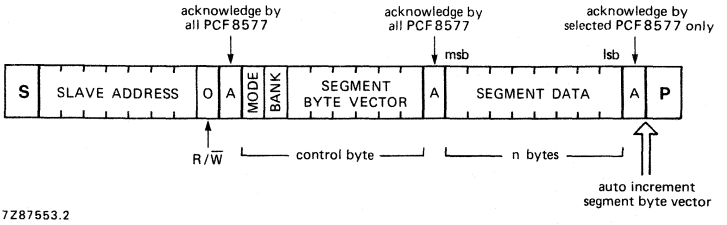


Fig. 15 I²C bus protocol.

The PCF8577 is a slave receiver and has a fixed slave address (Fig. 14). All PCF8577 on the same bus acknowledge the slave address in parallel. The second byte is always the control byte and is loaded into the control register of each PCF8577 on the bus. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a stop (P) condition is given after the control byte acknowledge the segment data remains unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data only the selected PCF8577 gives an acknowledge. Loading is terminated by generating a stop (P) condition.

DISPLAY MEMORY MAPPING

The mapping between the eight segment registers and the segment outputs S1 to S32 is shown in Tables 1 and 2.

Since only one register bit per segment is needed in the direct drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0 even bytes (BANK A) are displayed; if BANK is set to logic 1 odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct drive mode.

Table 1 Segment byte — segment driver mapping in the direct drive mode.

MODE	BANK	V2	V1	V0	SEGMENT REGISTER / BIT	MSB 7	6	5	4	3	2	1	LSB 0	BACKPLANE
0	0	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP1

Mapping example: bit 0 of register 7 controls the LCD segment S25 if BANK bit is a logic 1.

DISPLAY MEMORY MAPPING (continued)

Even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 2 Segment byte — segment driver mapping in the duplex mode.

MODE	BANK	V2	V1	V0	SEGMENT REGISTER / BIT	M S B 7	6	5	4	3	2	1	L S B 0	BACKPLANE
1	x	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
1	x	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP2
1	x	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
1	x	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP2
1	x	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
1	x	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP2
1	x	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
1	x	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP2

X = don't care.

Mapping example: bit 7 of register 5 controls the LCD segment S24/BP2.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to 11	V
Voltage on any pin	V_I	V_{SS} − 0,8 to V_{DD} + 0,8	V
D.C. input current	$\pm I_I$	max. 20	mA
D.C. output current	$\pm I_O$	max. 25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$, I_{SS}	max. 50	mA
Power dissipation per package	P_{tot}	max. 500*	mW
Power dissipation per output	P	max. 100	mW
Operating ambient temperature range	T_{amb}	−40 to +85	°C
Storage temperature range	T_{stg}	−65 to +150	°C

* Derate 7,7 mW/K when $T_{amb} > 60$ °C.

CHARACTERISTICS

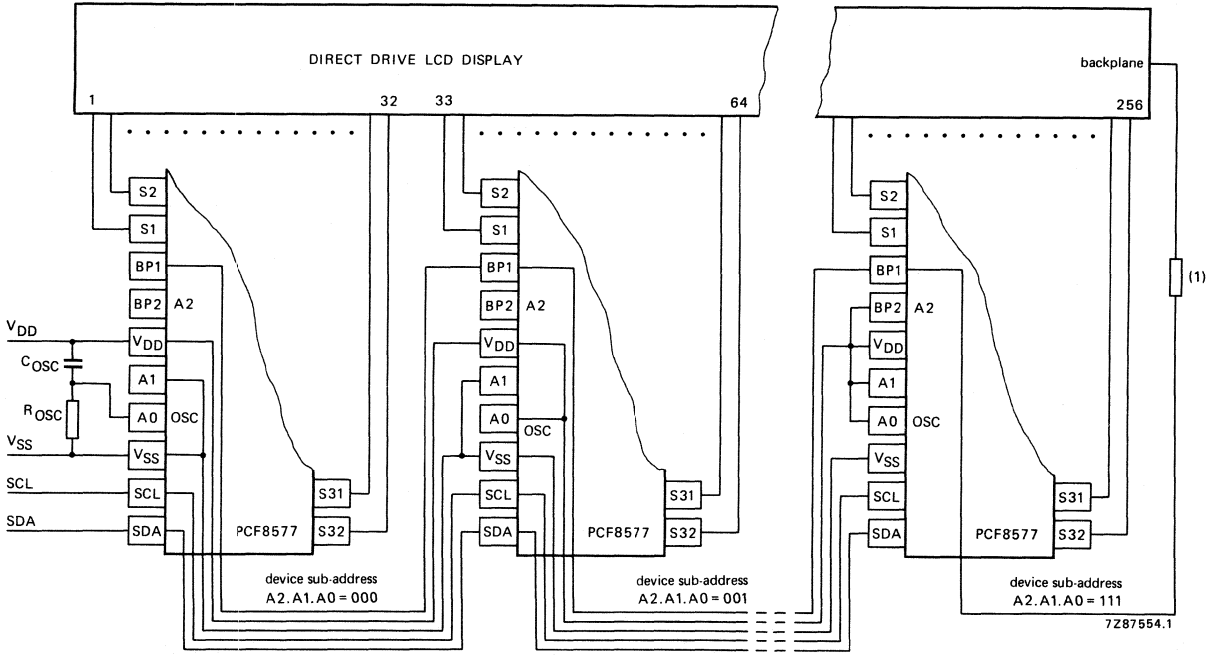
V_{DD} = 2,5 to 9 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.*	max.	unit
Supply voltage	V_{DD}	2,5	–	9,0	V
Supply current					
f_{SCL} = 100 kHz; no load; R_{OSC} = 1 MΩ	I_{DD}	–	80	250	μA
f_{SCL} = 0; no load; R_{OSC} = 1 MΩ; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD}	–	35	70	μA
Power-on-reset level**	V_{REF}	–	1,1	2,0	V
Input SCL; input/output SDA					
input voltage LOW	V_{IL}	0	–	0,8	V
input voltage HIGH	V_{IH}	2,0	–	9,0	V
output current LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA
output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
tolerable spike width on bus	t_{sw}	–	–	100	ns
input capacitance at $V_I = V_{SS}$	C_I	–	–	7	pF
A1 input leakage current at $V_I = V_{SS}$ or V_{DD}	I_I	–	–	250	nA
A2/BP2 input current at $V_I = V_{DD}$	I_I	–	2,0	–	μA
A0/OSC input current at $V_I = V_{SS}$ or V_{DD}	$\pm I_I$	–	5,0	–	μA
DC component of LCD driver	$\pm V_{BP}$	–	20	–	mV
Segment loads	C_{SX}	–	–	5	nF
	R_{SX}	1	–	–	MΩ
Segment output current at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL}	0,3	–	–	mA
Segment output current at $V_{OH} = V_{DD} - 0,4$ V; V_{DD} = 5 V	$-I_{OH}$	0,3	–	–	mA
Backplane load (direct drive)	C_{BP}	–	–	50	nF
	R_{BP}	100	–	–	kΩ
Backplane loads (duplex drive)	C_{BP}	–	–	35	nF
	R_{BP}	100	–	–	kΩ
Rise and fall times ($V_{BP} - V_{SX}$) at maximum load	t_r, t_f	–	–	200	μs
Display frequency at C_{OSC} = 680 pF; R_{OSC} = 1 MΩ	f_{LCD}	65	90	120	Hz

* V_{DD} = 5 V; T_{amb} = 25 °C.

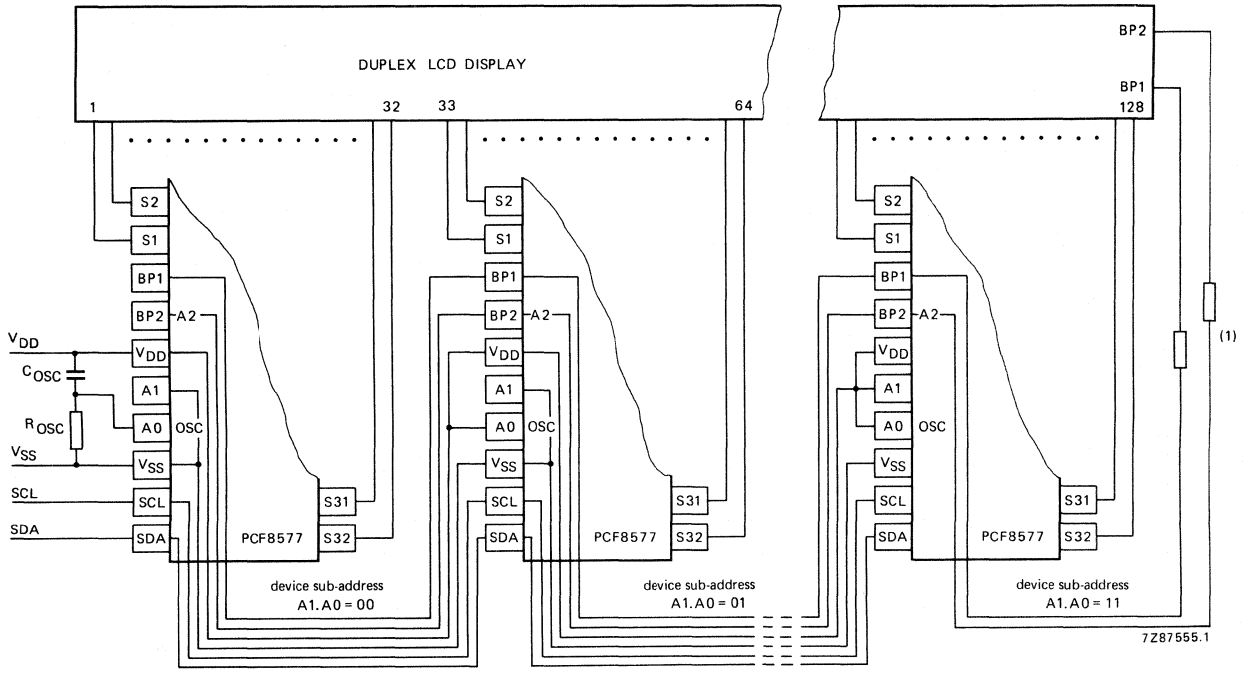
** The power-on-reset circuit resets the I²C bus logic with $V_{DD} < V_{REF}$.

APPLICATION INFORMATION



(1) The series resistance of the display backplane must be greater than 1 Ω.

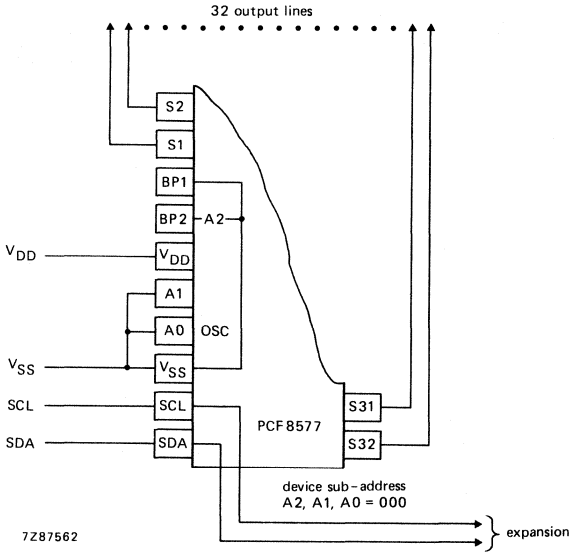
Fig. 16 Direct drive display; expansion to 256 segments using eight PCF8577.



(1) The series resistances of the display backplanes must be greater than 1 kΩ.

Fig. 17 Duplex display; expansion to 2 x 128 segments using four PCF8577.

APPLICATION INFORMATION (continued)



Notes

1. MODE bit must always be set to 0 (direct drive)
2. BANK switching is permitted
3. BP1 must always be connected to V_{SS} and A0/OSC must be connected to either V_{DD} or V_{SS} (no LCD modulation)

Fig. 18 Use of PCF8577 as 32-bit output expander in I²C bus application.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

FM RADIO CIRCUIT

GENERAL DESCRIPTION

The TDA7000 is a monolithic integrated circuit for mono FM portable radios, where a minimum on peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The i.f. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

The TDA7000 includes the following functions:

- R.F. input stage
- Mixer
- Local oscillator
- I.F. amplifier/limiter
- Phase demodulator
- Mute detector
- Mute switch

QUICK REFERENCE DATA

Supply voltage range (pin 5)	V_P	2,7 to 10	V
Supply current at V_P = 4,5 V	I_P	typ. 8	mA
R.F. input frequency range	f_{rf}	1,5 to 110	MHz
Sensitivity for −3 dB limiting (e.m.f. voltage) (source impedance: 75 Ω; mute disabled)	EMF	typ. 1,5	μV
Signal handling (e.m.f. voltage) (source impedance: 75 Ω)	EMF	typ. 200	mV
A.F. output voltage at R_L = 22 kΩ	V_o	typ. 75	mV

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

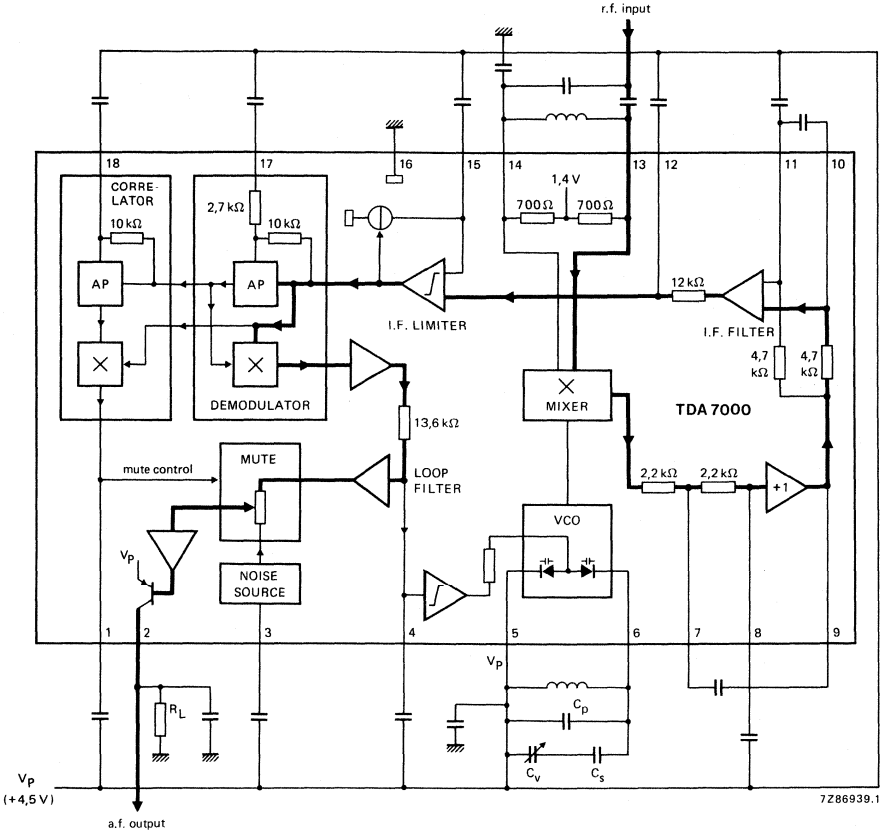


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 5)	V_P	max.	12 V
Oscillator voltage (pin 6)	V_{6-5}	V_P–0,5 to V_P +0,5	V
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		0 to + 60 °C

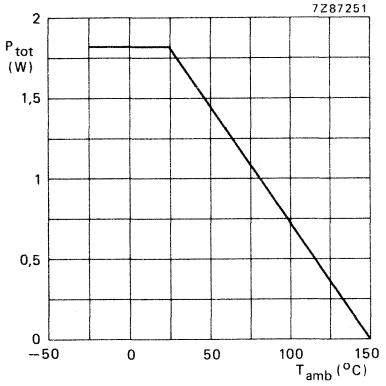


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 5)	V_P	2,7	4,5	10	V
Supply current at V_P = 4,5 V	I_P	–	8	–	mA
Oscillator current (pin 6)	I_6	–	280	–	μA
Voltage at pin 14	V_{14-16}	–	1,35	–	V
Output current at pin 2	I_2	–	60	–	μA
Voltage at pin 2; R_L = 22 kΩ	V_{2-16}	–	1,3	–	V

A.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4 (mute switch open, enabled); f_{rf} = 96 MHz (tuned to max. signal at 5 μV e.m.f.) modulated with Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 0,2 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Sensitivity (see Fig. 3) (e.m.f. voltage)					
for −3 dB limiting; muting disabled	EMF	–	1,5	–	μV
for −3 dB muting	EMF	–	6	–	μV
for S/N = 26 dB	EMF	–	5,5	–	μV
Signal handling (e.m.f. voltage) for THD < 10%; Δf = ± 75 kHz	EMF	–	200	–	mV
Signal-to-noise ratio	S/N	–	60	–	dB
Total harmonic distortion					
at Δf = ± 22,5 kHz	THD	–	0,7	–	%
at Δf = ± 75 kHz	THD	–	2,3	–	%
AM suppression of output voltage (ratio of the AM output signal referred to the FM output signal) FM signal: f_m = 1 kHz; Δf = ± 75 kHz AM signal: f_m = 1 kHz; m = 80%	AMS	–	50	–	dB
Ripple rejection (ΔV_P = 100 mV; f = 1 kHz)	RR	–	10	–	dB
Oscillator voltage (r.m.s. value) at pin 6	$V_{6\text{-}5(rms)}$	–	250	–	mV
Variation of oscillator frequency with supply voltage (ΔV_P = 1 V)	Δf_{osc}	–	60	–	kHz/V
Selectivity	S_{+300}	–	45	–	dB
	S_{-300}	–	35	–	dB
A.F.C. range	Δf_{rf}	–	± 300	–	kHz
Audio bandwidth at ΔV_o = 3 dB measured with pre-emphasis (t = 50 μs)	B	–	10	–	kHz
A.F. output voltage (r.m.s. value) at R_L = 22 kΩ	$V_{o(rms)}$	–	75	–	mV
Load resistance					
at V_P = 4,5 V	R_L	–	–	22	kΩ
at V_P = 9,0 V	R_L	–	–	47	kΩ

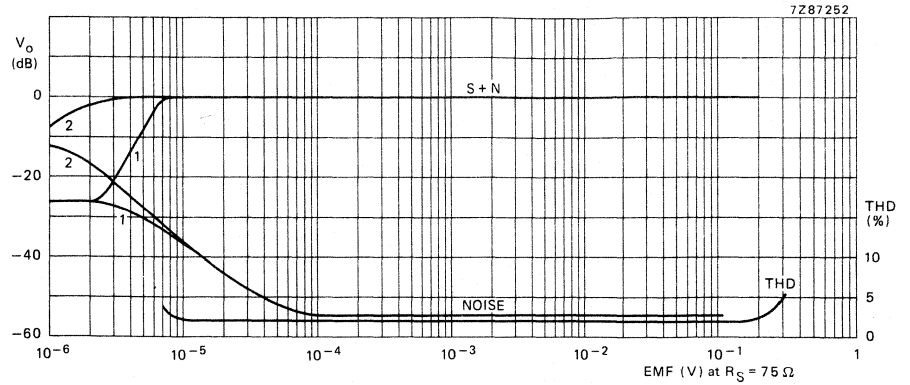


Fig. 3 A.F. output voltage (V_o) and total harmonic distortion (THD) as a function of the e.m.f. input voltage (EMF) with a source impedance (R_S) of 75 Ω: (1) muting system enabled; (2) muting system disabled.

Conditions: 0 dB = 75 mV; f_{rf} = 96 MHz.
for S + N curve: Δf = ± 22,5 kHz; f_m = 1 kHz.
for THD curve: Δf = ± 75 kHz; f_m = 1 kHz.

Notes

1. The muting system can be disabled by feeding a current of about 20 μA into pin 1.
2. The interstation noise level can be decreased by choosing a low-value capacitor at pin 3. Silent tuning can be achieved by omitting this capacitor.

DEVELOPMENT SAMPLE DATA

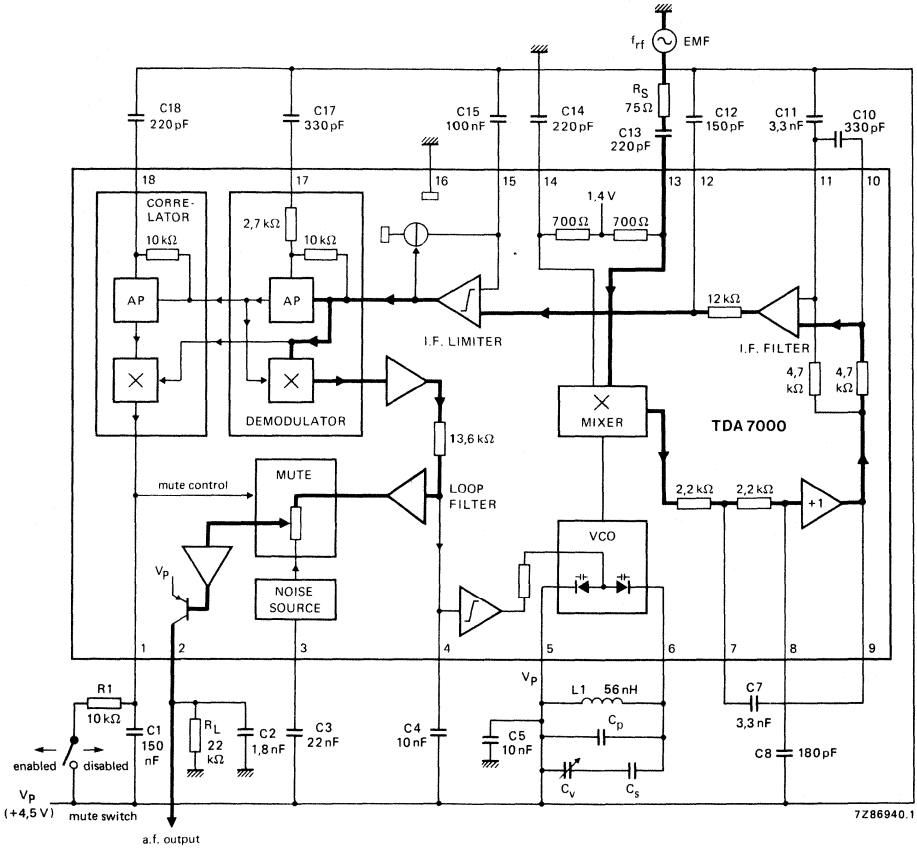


Fig. 4 Test circuit; for printed-circuit boards see Figs 5 and 6.

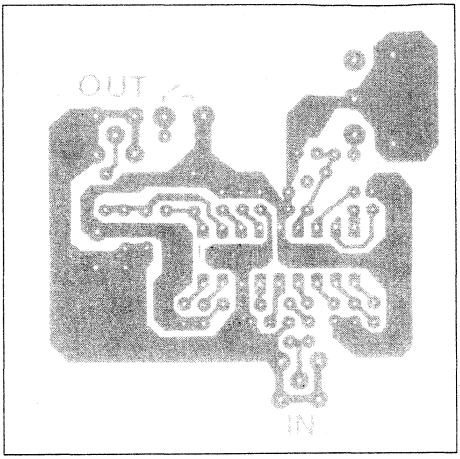


Fig. 5 Track side of printed-circuit board used for the circuit of Fig. 4.

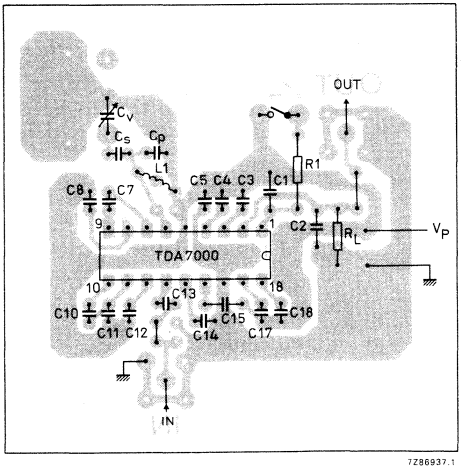


Fig. 6 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0		V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ.	3,2	mA
Bridge tied load application (BTL)				
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ.	140	mW
D.C. output offset voltage between the outputs	$\lvert\Delta V\rvert$	max.	70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	140	μV
Stereo application				
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ.	35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ.	75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ.	40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	100	μV

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO-8; SOT-96A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

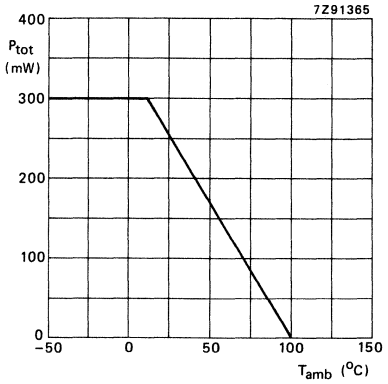


Fig. 1 Power derating curve.

SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{j\,max} - T_{amb}}{R_{th\,j\text{-}a}} = \frac{100-60}{300} = 0{,}1\ \text{W}.$$

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	–	26	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

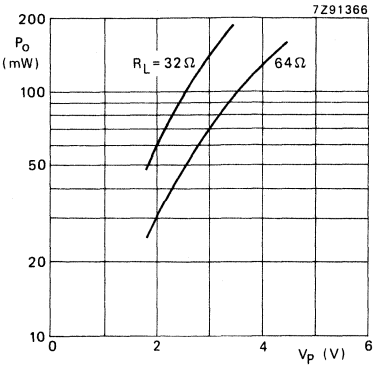


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

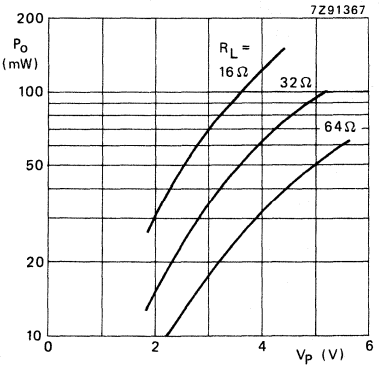


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

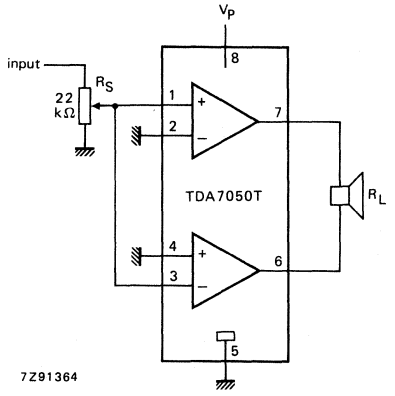


Fig. 4 Application diagram (BTL); also used as test circuit.

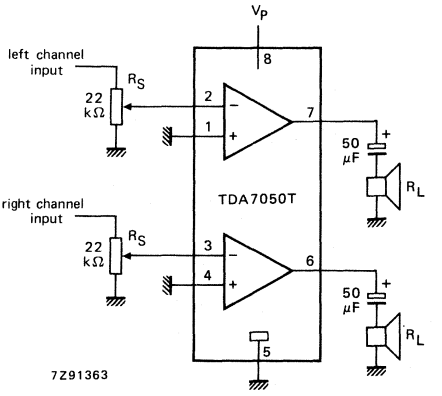


Fig. 5 Application diagram (stereo); also used as test circuit.

TELEPHONE TRANSMISSION CIRCUIT FOR HANDSFREE LOUDSPEAKING

GENERAL DESCRIPTION

The TEA1042 is a bipolar integrated circuit performing all speech and line interface functions in electronic telephone sets. It is especially designed for handsfree loudspeaking equipment.

Its features are:

- Supplied from telephone line current
- Voltage regulator with adjustable d.c. voltage drop and d.c. resistance
- High and low-impedance handset microphone inputs
- High-impedance base microphone input
- Handset/base selection input
- Muting input for pulse or DTMF dialling
- Gain setting facility on all amplifiers
- Line current dependent gain control facility with corrections for the exchange supply voltage and its feeding bridge resistance
- Supply output for additional circuits.

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{line}	typ.	4,2 V
Line current operating range	I_{line}		10 to 140 mA
Telephone line impedance	$\|Z_{line}\|$	nom.	600 Ω
Supply current	I_{CC}	typ.	1 mA
Voltage gain, transmitting amplifier			
MIC1 input	A_{vd}	typ.	44,1 dB
MIC2 input	A_{vd}	typ.	20 dB
MIC3 input	A_{vd}	typ.	20 dB
DTMF input	A_{vd}	typ.	25,6 dB
Voltage gain, receiving amplifier	A_{vd}	typ.	27 dB
Gain adjustment range			
transmitting amplifier	ΔA_{vd}	typ.	± 6 dB
receiving amplifier	ΔA_{vd}	typ.	± 8 dB
Range of gain control with line current, all amplifiers	ΔA_{vd}	typ.	6 dB
Exchange supply voltage range	V_{exch}		24 to 60 V
Exchange feeding bridge resistance	R_{exch}		400 or 800 Ω
Operating ambient temperature range	T_{amb}		−25 to + 70 °C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

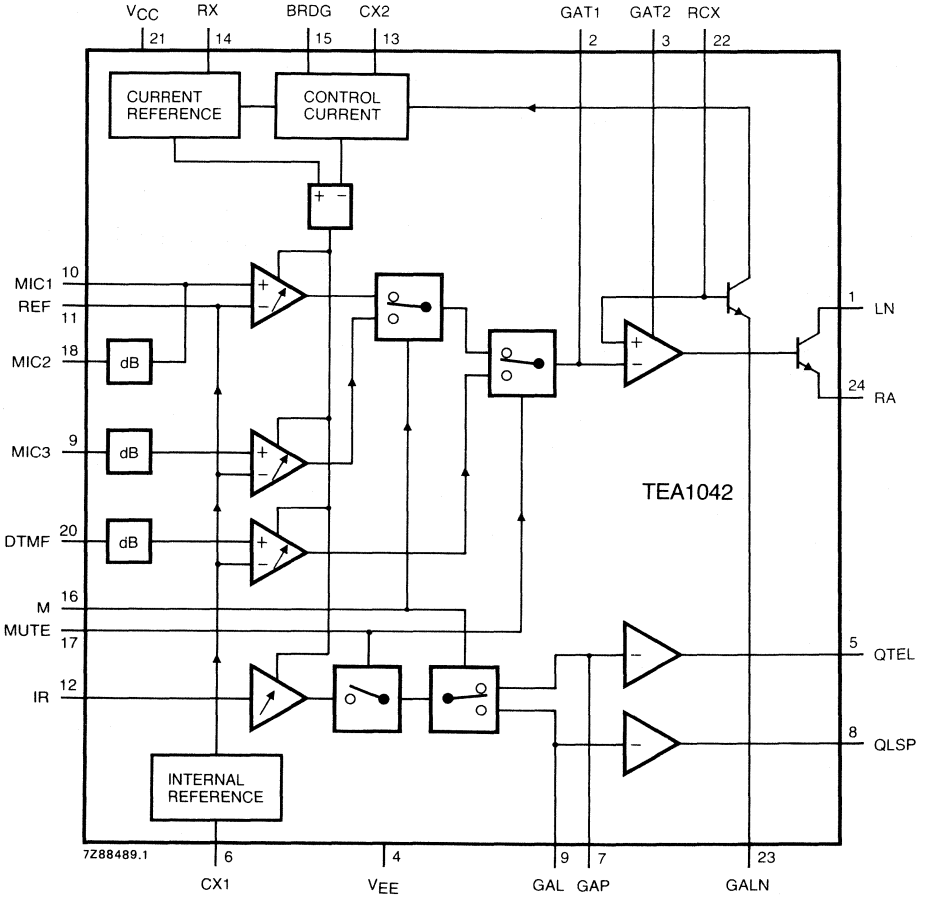


Fig. 1 Block diagram. The blocks marked dB are attenuators. The M and MUTE inputs operate analogue switches that activate or inhibit the inputs and outputs as required by their function.

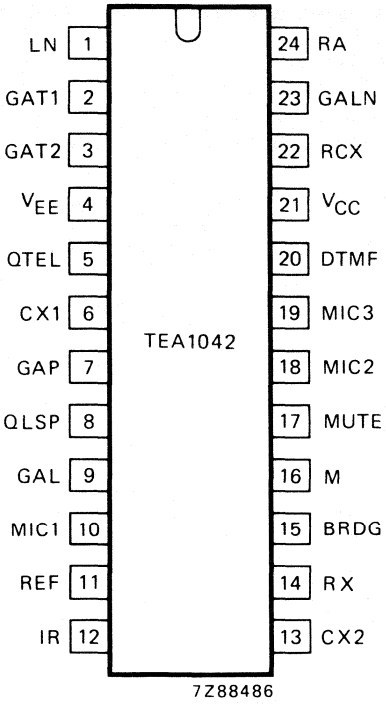


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAT1	gain adjustment; transmitting amplifier
3	GAT2	gain adjustment; transmitting amplifier
4	V_{EE}	negative line terminal
5	QTEL	handset telephone output
6	CX1	reference decoupling
7	GAP	gain adjustment; telephone amplifier
8	QLSP	loudspeaker preamplifier output
9	GAL	gain adjustment; loudspeaker preamplifier
10	MIC1	low-impedance handset microphone input
11	REF	reference voltage
12	IR	receiving amplifier input
13	CX2	external stabilizing capacitor
14	RX	external resistor
15	BRDG	selection input for gain control adaptation to feeding bridge impedance
16	M	mode (handset/base selection) input
17	MUTE	mute input
18	MIC2	high-impedance handset microphone input
19	MIC3	base microphone input
20	DTMF	dual-tone multi-frequency input
21	V_{CC}	positive supply
22	RCX	line voltage adjustment and voltage regulator decoupling
23	GALN	gain control with line current; all amplifiers
24	RA	d.c. resistance adjustment

FUNCTIONAL DESCRIPTION

The TEA1042 contains two receiving amplifiers, a transmitting amplifier, means to switch the inputs and the outputs, means to adjust the gain of all amplifiers individually, means to vary the gain with the line current and means to adjust the d.c. voltage drop and d.c. resistance. See the block diagram, Fig. 1.

Supply: LN, V_{CC}, V_{EE}, RA, CX1 and CX2 (pins 1, 21, 4, 24, 6 and 13)

The circuit is supplied from the line current, the arrangement is shown in Fig. 3. The circuit develops its own supply voltage at V_{CC} (pin 21). This supply voltage may also be used to supply an external circuit, e.g. a CMOS pulse or DTMF dialler or an electret microphone amplifier stage. The current available for this circuit depends on external components, see Fig. 4.

All line current has to flow through the circuit. If the line current exceeds the current required by the circuit itself via V_{CC} (pin 21), i.e. about 1 mA, plus the current required by the peripheral circuits connected to this pin, then the excess current is diverted via LN, the positive line terminal (pin 1), to RA (d.c. resistance adjustment; pin 24).

The minimum line voltage may be chosen by external resistor R5 and the variation with line current by external resistor R10. The circuit regulates the line voltage at $T_{amb} = 25\ ^{o}C$ to:

$$V_{line} = V_{LN} = \frac{R5 + R9}{R9} \times 0{,}62 + I_{LN} \times R10,$$

I_{LN} being the current diverted via LN.

A regulator decoupling capacitor has to be connected between RCX (pin 22) and V_{EE}, the negative line terminal (pin 4), a smoothing capacitor has to be connected between V_{CC} (pin 21) and V_{EE}, and a stabilizing capacitor between CX2 (pin 13) and V_{EE}. Further a decoupling capacitor has to be connected between CX1 (reference decoupling; pin 6) and V_{EE} (pin 4).

The dynamic impedance that the circuit presents to the line in the speech band is determined primarily by resistor R1 connected between LN (pin 1) and V_{CC} (pin 21).

Mode (handset/base selection) input M (pin 16)

The mode input permits selection of operation via the handset or via the base. A HIGH level on the M input or an open circuit selects handset operation, i.e. it activates the microphone inputs MIC1 and MIC2 and the handset telephone output QTEL. A LOW level on M selects the base microphone input MIC3 and the loudspeaker preamplifier output QLSP.

Microphone inputs MIC1, MIC2 and MIC3 (pins 10, 18 and 19)

Handset and base may be equipped with a sensitive microphone, e.g. an electret microphone with pre-amplifier. This has to be connected to the MIC2 or MIC3 input respectively. The available gain from these inputs is typ. 20 dB.

The handset may also be equipped with an insensitive low-impedance microphone, e.g. a dynamic or magnetic microphone. This has to be connected between MIC1 (pin 10) and (REF (pin 11). The available gain from this input is typ. 44,1 dB.

Dual-tone multi-frequency input DTMF and mute input MUTE (pins 20 and 17)

A HIGH level on the MUTE input inhibits all microphone inputs and the telephone and loudspeaker outputs QTEL and QLSP and enables the DTMF input, a LOW level does the reverse. Switching the MUTE input will not produce any clicks on the line or in the telephone or loudspeaker. The available gain from the DTMF input is typ. 25,6 dB.

Telephone output QTEL and loudspeaker preamplifier output QLSP (pins 5 and 8)

As described before, the M input determines which of the outputs QTEL and QLSP will be activated. The receiving amplifier input IR (pin 12) is the input for both outputs. For both outputs the available gain is typ. 27 dB. The output QTEL is intended for telephone capsules with an impedance of 150 Ω or more. The QLSP output is intended to drive a power amplifier. Its output impedance is less than 1 kΩ.

Gain adjustment: GAT1, GAT2, GAP and GAL (pins 2, 3, 7 and 9)

The gain of the transmitting amplifier may be adjusted by an external resistor R2 connected between GAT1 and GAT2 (pins 2 and 3; see Fig. 9). This adjustment influences the sensitivity of the inputs MIC1, MIC2, MIC3 and DTMF to the same amount. The gain is proportional to R2 and inversely proportional to R10 and R12.

The gain of the telephone amplifier may be adjusted by an external resistor R14 between GAP (pin 7) and CX1 (pin 6). The gain is proportional to R14 and inversely proportional to R12.

The gain of the loudspeaker preamplifier may be adjusted by an external resistor R13 between GAL (pin 9) and CX1 (pin 6). The gain is proportional to R13 and inversely proportional to R12.

Gain control with line current: GALN (pin 23)

The circuit offers a facility to automatically vary the gain of all its amplifiers with the line current. In this way the circuit compensates for differences in line attenuation. The variation is accomplished by connecting an external resistor R11 between GALN (pin 23) and V_{EE} (pin 4). The value of this resistor should be chosen in accordance with the supply voltage of the exchange (see Figs 5 and 6).

If no gain variation with line current is required the GALN connection may be left open. All amplifiers have their maximum gain then.

Selection input for gain control adaptation to feeding bridge impedance: BRDG (pin 15)

A LOW level at the BRDG input optimizes the gain control characteristics of the circuit for a 400 Ω feeding bridge in the exchange, a HIGH level for 800 Ω.

Side tone suppression

In the circuit diagram shown in Fig. 9 side tone suppression is obtained with components C2, R3, R4, R7 and R8. Their component values have to be chosen to suit the cable type used. This network attenuates the signal from the telephone line to the IR input of the receiving amplifier. This attenuation may be adjusted by choosing the value of R7 without affecting the side tone suppression.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current			
d.c.	I_{line}	max.	140 mA
non-repetitive ($t < 100$ h)	I_{line}	max.	250 mA
Storage temperature range	T_{stg}	−40 to +125	°C
Operating ambient temperature range	T_{amb}	−25 to +70	°C
Junction temperature	T_j	max.	150 °C

CHARACTERISTICS

I_{line} = 10 to 140 mA; f = 1000 Hz; T_{amb} = 25 °C, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 21)					
Line voltage					
I_{line} = 15 mA	V_{line}	4	4,2	4,4	V
I_{line} = 50 mA	V_{line}	–	–	5,8	V
I_{line} = 100 mA	V_{line}	–	–	7,3	V
Variation with temperature	$-\Delta V_{line}/\Delta T$	8	10	12	mV/K
Line current operating rage	I_{line}	10	–	140	mA
Supply current at V_{CC} = 2 V	I_{CC}	–	–	1	mA
Mode (handset/base selection) input M (pin 16)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{16}$	–	8	20	μA
Attenuation of non-selected signals	$-\Delta A_{vd}$	45	–	–	dB
Low-impedance handset microphone input MIC1 and reference voltage pin REF (pins 10 and 11)					
Input impedance	$\lvert Z_{10\text{-}11}\rvert$	–	3	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	43,1	44,1	45,1	dB
High-impedance handset microphone input MIC2 (pin 18)					
Input impedance	$\lvert Z_{18\text{-}4}\rvert$	40	48	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	19	20	21	dB
Base microphone input MIC3 (pin 19)					
Input impedance	$\lvert Z_{19\text{-}4}\rvert$	40	48	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	19	20	21	dB
DTMF input (pin 20)					
Input impedance	$\lvert Z_{20\text{-}4}\rvert$	10	15	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	24,6	25,6	26,6	dB
Gain adjustment pins; transmitting amplifier: GAT1 and GAT2 (pins 2 and 3)					
Gain adjustment range	ΔA_{vd}	–	± 6	–	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = −5 to +45 °C	ΔA_{vd}	–	± 0,5	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Transmitting amplifier output LN (pin 1)					
Output voltage at I_{line} = 15 mA; R_{line} = 600 Ω; d = 2%	$v_{LN(rms)}$	1,4	–	–	V
Psophometrically weighted* noise output voltage at I_{line} = 15 mA; R_{line} = 600 Ω	$v_{LN(rms)}$	–	245	–	μV
MUTE input (pin 17)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{17}$	–	8	20	μA
Attenuation of non-selected signals	$-\Delta A_{vd}$	45	–	–	dB
Receiving amplifier input IR (pin 12)					
Input impedance	$\lvert Z_{12\text{-}4}\rvert$	–	10	–	kΩ
Telephone output QTEL (pin 5)					
Voltage gain at I_{line} = 15 mA; R_{load} = 150 Ω; R13 = 15 kΩ; see Fig. 8	A_{vd}	26	27	28	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	±0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = −5 to +45 °C	ΔA_{vd}	–	±0,5	–	dB
Maximum output voltage at I_{line} = 15 mA; R_{load} = 150 Ω; d = 2%	$v_{O(rms)}$	350	–	–	mV
Psophometrically weighted* noise output voltage at I_{line} = 15 mA	$v_{O(rms)}$	–	40	–	μV
Gain adjustment pin; telephone amplifier: GAP (pin 7)					
Gain adjustment range	ΔA_{vd}	–	±8	–	dB
Loudspeaker preamplifier output QLSP (pin 8)					
Voltage gain at I_{line} = 15 mA; R_{load} = 10 kΩ; R14 = 15 kΩ; see Fig. 8	A_{vd}	–	27	–	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	±0,5	–	dB
Gain variation with temperature	ΔA_{vd}	–	±0,5	–	dB
Psophometrically weighted* noise output voltage at I_{line} = 15 mA	$v_{O(rms)}$	–	40	–	μV
Output impedance	$\lvert Z_{8\text{-}4}\rvert$	–	–	1	kΩ
Gain adjustment pin; loudspeaker preamplifier: GAL (pin 9)					
Gain adjustment range	ΔA_{vd}	–	±8	–	dB

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Selection input for gain control adaptation to feeding bridge impedance BRDG (pin 15)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{15}$	–	8	20	μA
Gain control with line current pin GALN (pin 23)					
Gain control range	ΔA_{vd}	–	6	–	dB
Highest line current for maximum gain, R11 = 105 kΩ;					
BRDG = HIGH (R_{exch} = 800 Ω)	I_{line}	22,5	25	27,5	mA
BRDG = LOW (R_{exch} = 400 Ω)	I_{line}	31,5	35	38,5	mA
Lowest line current for minimum gain, R11 = 105 kΩ;					
BRDG = HIGH (R_{exch} = 800 Ω)	I_{line}	49,5	55	60,5	mA
BRDG = LOW (R_{exch} = 400 Ω)	I_{line}	81	90	99	mA

* P53 curve.

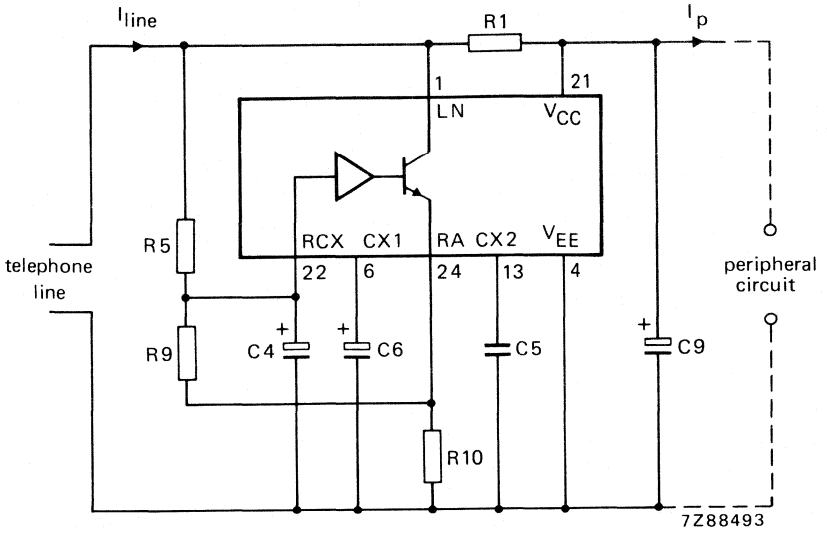


Fig. 3 Supply arrangement.

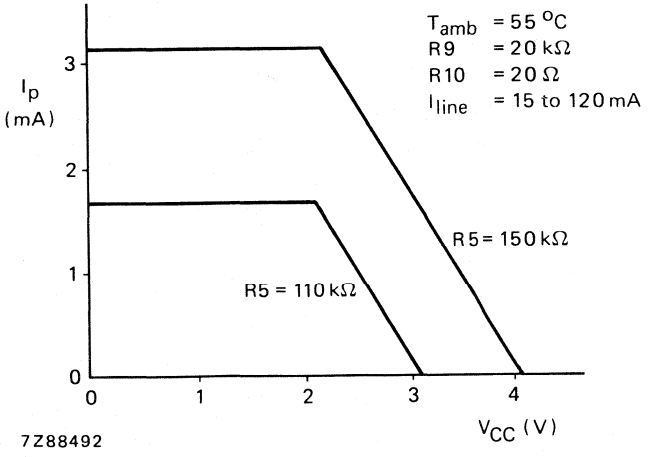


Fig. 4 Maximum current I_p available from V_{CC} for external (peripheral) circuits.

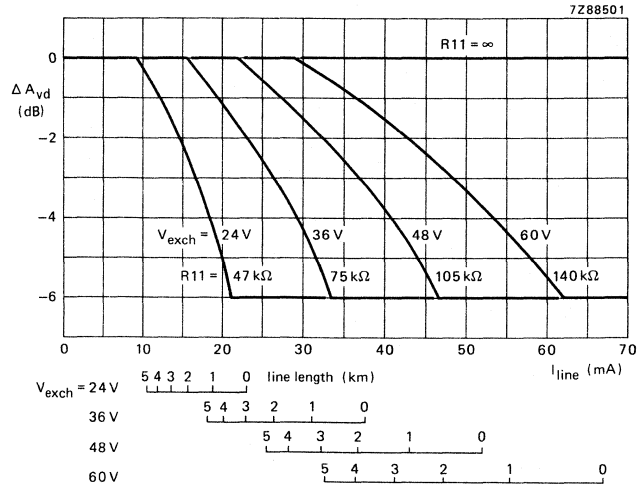


Fig. 5 Gain variation with line current, with R11 as a parameter, and with the BRDG input HIGH, i.e. the circuit optimized for 800 Ω. The values chosen for R11 suit the usual values for the supply voltage of the exchange. The curves are valid for 0,5 mm twisted-pair cables with an attenuation of 1,2 dB/km and a d.c. resistance of 176 Ω/km.

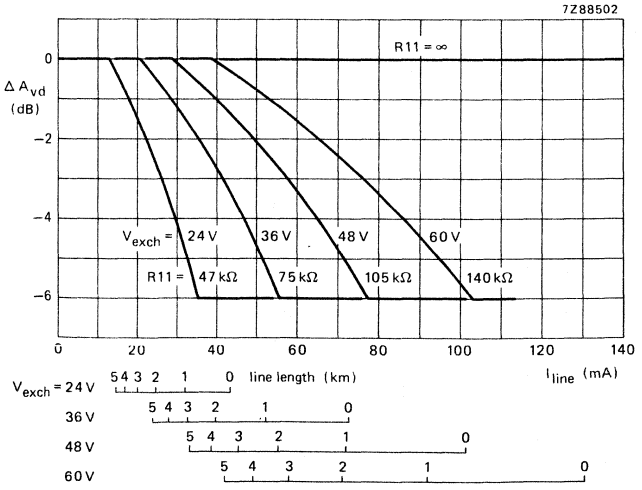


Fig. 6 Gain variation with line current, with R11 as a parameter, and with the BRDG input LOW, i.e. the circuit optimized for 400 Ω. The values chosen for R11 suit the usual values for the supply voltage of the exchange. The curves are valid for 0,5 mm twisted-pair cables with an attenuation of 1,2 dB/km and a d.c. resistance of 176 Ω/km.

DEVELOPMENT SAMPLE DATA

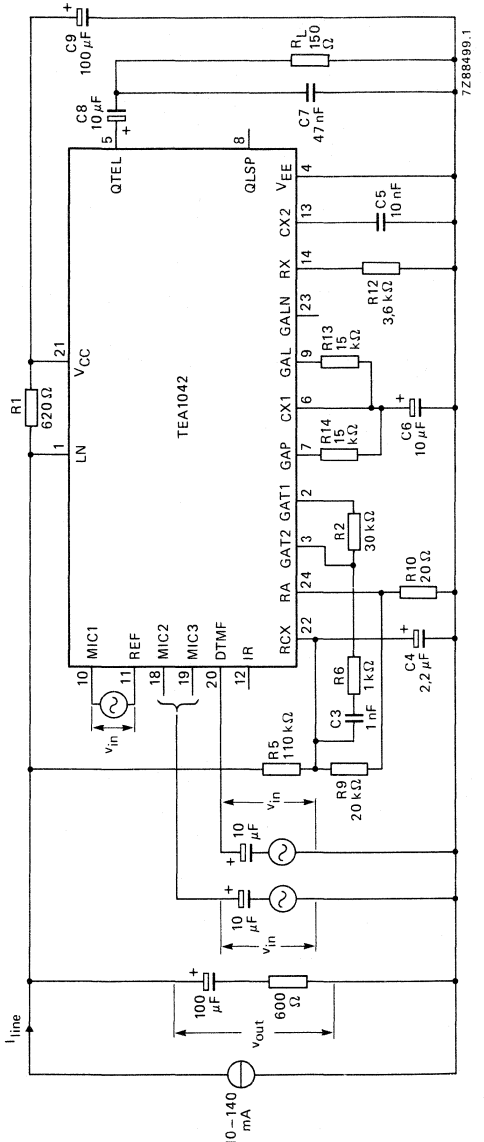


Fig. 7 Test circuit for defining voltage gain of MIC1, MIC2, MIC3 and DTMF inputs. Gain is defined as: $A_{vd} = 20 \log |v_{out}/v_{in}|$. For measuring the MIC1 or MIC2 input the M input should be HIGH and the MUTE input LOW, for measuring the MIC3 input M and MUTE should both be LOW and for measuring the DTMF input M and MUTE should be HIGH. Inputs not under test should be open.

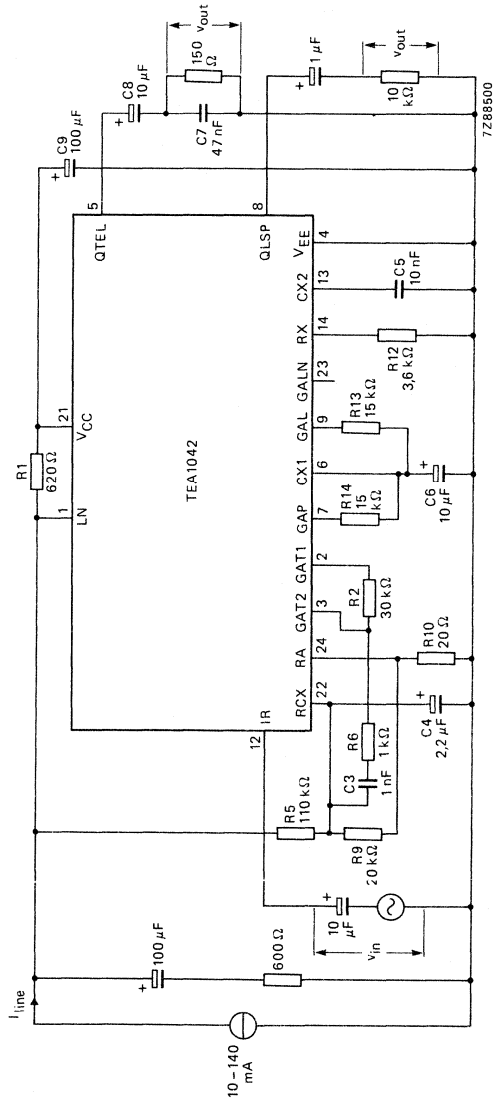


Fig. 8 Test circuit for defining voltage gain of QTEL and QLSP outputs. Gain is defined as: $A_{vd} = 20 \log |v_{out}/v_{in}|$. For measuring the QTEL output the M input should be HIGH and the MUTE input LOW, for measuring the QLSP output M and MUTE should both be LOW.

DEVELOPMENT SAMPLE DATA

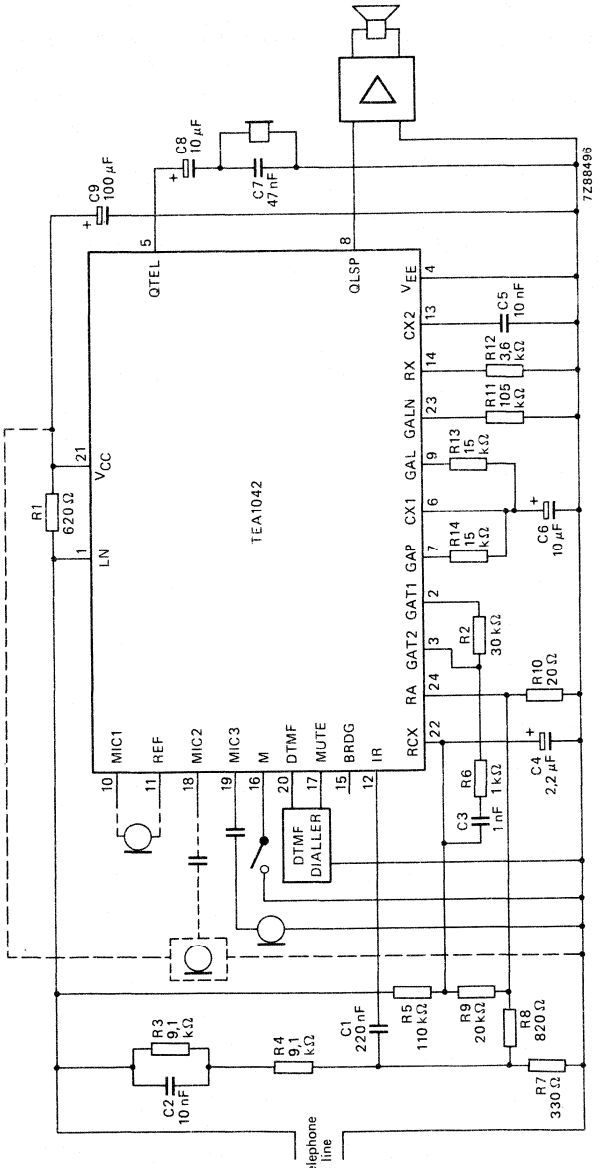


Fig. 9 Typical application of the TEA1042 in an electronic handsfree telephone set. The connections to the MIC1 and MIC2 inputs are alternatives. The connection to the BRDG input is not shown, see the Functional Description. The diagram does not show voice switches and associated control circuits required in a practical circuit for stable loudspeaking operation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

DTMF/SPEECH TRANSMISSION INTEGRATED CIRCUIT FOR TELEPHONE APPLICATIONS

This integrated circuit is a dual-tone multi-frequency (DTMF) generator and a speech transmission circuit on a single chip. It supplies frequency combinations in accordance with CCITT recommendations for use in push-button telephones. It can be operated with a single contact keyboard or via a direct interface with a microcomputer. I^2L technology allows digital and analogue functions to be implemented on the same chip.

The speech-transmission part incorporates microphone and telephone amplifiers, anti-sidetone and line adaption. The microphone inputs, suitable for different types of transducer, are symmetrical to allow long cable connections with good immunity against radio-frequency interference.

The logic inputs contain an interface circuit to guarantee well defined states and on and off resistance of the keyboard contacts.

Features

- stabilized DTMF levels to be set externally
- wide operating range of line current and temperature
- no individual DTMF level adjustments required
- microcomputer compatible logic inputs
- gain setting for microphone and receiver amplifiers
- internally generated electronic muting
- low spreads on amplifier gains
- low number of external components
- on-chip oscillator for 3,58 MHz crystal

QUICK REFERENCE DATA

Line voltage	V_L	typ. 4,8	V
Line current	I_L	10 to 120	mA
Adjustable dynamic resistance	R_i	600 to 900	Ω
Microphone signal amplification	A_M	typ. 50	dB
Receiver signal amplification	A_T	typ. 20	dB
DTMF tone levels (adjustable)			
lower tones	V_{LG}	max. −6	dBm
higher tones	V_{HG}	max. −4	dBm
Operating temperature range	T_{amb}	−25 to +70	°C

PACKAGE OUTLINES

TEA1046P: 24-lead DIL, plastic (SOT-101).

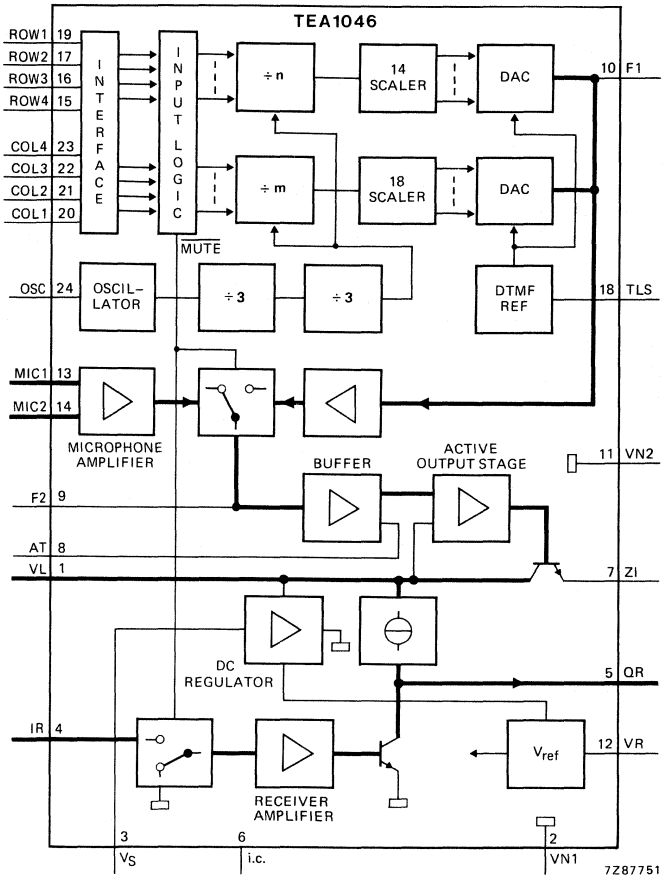


Fig. 1 Functional block diagram.

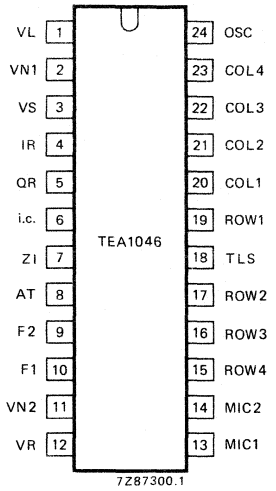


Fig. 2 Pinning diagram.

PINNING

1	VL	positive line voltage
2	VN1	negative line voltage
3	VS	voltage stabilizer filter
4	IR	receiver amplifier input
5	QR	receiver amplifier output
6	i.c.	internally connected
7	ZI	impedance setting input
8	AT	anti-sidetone output
9	F2	second filter
10	F1	first filter
11	VN2	negative line voltage
12	VR	reference voltage output
13	MIC1	microphone input (pos.)
14	MIC2	microphone input (neg.)
15	ROW4	row input 941 Hz/BCD input
16	ROW3	row input 852 Hz/BCD input
17	ROW2	row input 770 Hz/BCD input
18	TLS	DTMF level setting
19	ROW1	row input 697 Hz/BCD input
20	COL1	column input 1209 Hz/mute input
21	COL2	column input 1336 Hz/mute input
22	COL3	column input 1477 Hz/enable input
23	COL4	column input 1633 Hz/mute input
24	OSC	oscillator input

FUNCTIONAL DESCRIPTION

Voltage regulator (Fig. 3)

Different line lengths and feeding bridge resistances of the exchange cause a large line current range to supply this circuit. As all functions on this chip are working within a total current of 10 mA, the rest of the line current is shunted by the voltage regulator circuit. It regulates the voltage drop over the circuit on a nominal level of 4,8 V.

The capacitor connected to input VS provides a low-pass filter function to avoid influence of the audio signals on the line.

The static behaviour of the voltage regulator is expressed by:

$$V_L = V_o + (I_L - I_i)\ R13$$

where V_o = 4,8 V at T_{amb} = 25 °C and R13 = 5 Ω, I_i = 10 mA.

The dynamic impedance of the regulator is equivalent to a resistor in series with a simulated inductor:

$$Zr\ (\omega) = R_{eq} + j\omega L_{eq}$$

where R_{eq} = R13 = 5 Ω

$L_{eq} \approx 5$ H ($C_{VS} \doteq 68\ \mu$F).

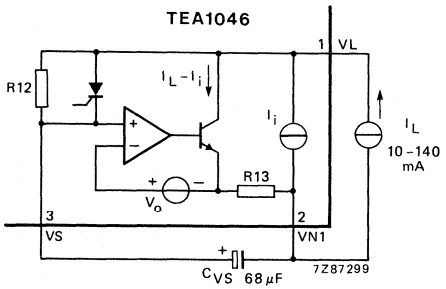


Fig. 3 Voltage regulator principle.

Within limited values, the d.c. level V_L can be decreased by connecting a resistor in parallel with R12, or increased by connecting a resistor in parallel with C_{VS}. The shunt regulator contains a thyristor which short-circuits R12 for a short period during switch-on time; this reduces the overshoot voltage to only 1 V above the level set by the regulator.

Active output stage

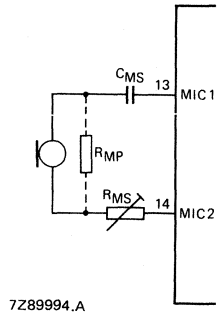
The amplifier consists of a voltage to current converter with a class-A output stage. Because of the feedback from the line to the input the circuit acts as a dynamic resistance (R_a). This resistance can be adjusted by the external resistor R_{ZI} (Fig. 11) and the value can be found by:

$$R_a = 8{,}93 \times R_{ZI}\ (\Omega)$$

The total dynamic resistance R_i equals R_a parallel with the resistance R_P of all other circuits parts, which value is approximately 7 kΩ.
With R_{ZI} = 75 Ω, R_a = 670 Ω and R_i = 610 Ω.
For R_{ZI} = 120 Ω, R_a = 1070 Ω and R_i = 900 Ω.

Microphone amplifier (Figs 4 and 5)

Pins 13 and 14 respectively are the non-inverting and inverting inputs for the microphone. The purely symmetrical inputs are suitable for low ohmic dynamic or magnetic capsules. The input impedance equals 4 kΩ. The voltage amplification from microphone input to pin 1 (VL) is 50 dB and if a lower gain is required the attenuation for a series resistor R_{MS} will be:

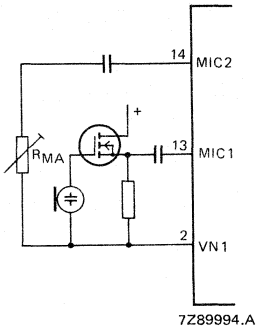


$$\frac{A_M(R_{MS} \neq 0)}{A_M(R_{MS} = 0)} = \frac{4}{4 + R_{MS}} \qquad (R_{MS} \text{ in k}\Omega)$$

$$A_M = \left| \frac{V_L}{V_M} \right|$$

Fig. 4 Symmetrical microphone connection. Resistor R_{MP} may be used to lower the microphone termination resistance.

The microphone amplifier also has an excellent behaviour for connection of an electret microphone with built in FET-source follower. In this condition pin 14 is decoupled for a.c. and the amplifier is driven at pin 13. The input impedance in this asymmetrical mode is 22 kΩ. If attenuation of the amplification is required the value of R_{MA} is given by:



$$\frac{A_M(R_{MA} \neq 0)}{A_M(R_{MA} = 0)} = \frac{22 + R_{MA}}{22 + 11R_{MA}} \quad (R_{MA} \text{ in k}\Omega)$$

$$A_M = \left| \frac{V_L}{V_{MIC1}} \right|$$

Fig. 5 Electret microphone circuit.

Receiver amplifier and anti-sidetone network (Fig. 14)

This amplifier is a non-inverting, fixed feedback amplifier with a class-A output stage. The gain is fixed and measures 20 dB from pin 4 (IR) to pin 5 (QR). The output is intended to drive dynamic capsules of nom. 220 Ω. For capsule impedances (Z_T) less than 220 Ω the maximum output voltage swing is determined by Z_T and the bias current of 3,9 mA. For Z_T greater than 220 Ω the maximum voltage swing is determined and soft-limited internally. The received line signal is attenuated by the anti-sidetone network an can be adjusted using R_{AT}. The amplification from the line to the telephone output is given by:

$$A_T = 10 \frac{R_{AT}}{R_{AT} + Z_S} \times \frac{Z_T}{Z_T + R_O}$$

Z_S is the impedance of the anti-sidetone network
Z_T is the capsule impedance
R_O is the amplifier output resistance

Optimum side-tone suppression is obtained as Z_S (R_{A1}, R_{A2} and C_A) equals

$$Z_S = K \frac{Z_L \times R_i}{Z_L + R_i}$$

Z_L = line terminating impedance
R_i = output stage impedance // passive circuit impedance
K = 200

In the application of Fig. 14 the network is optimized for 2 km of twisted copper wire (ϕ0,5 mm) cable with a d.c. resistance of 176 Ω/km. The side-tone suppression in the range from 0 to 10 km is at least 10 dB compared with the case when no compensation is applied.

Keyboard inputs

Inputs for the logic control are compatible with different types of keyboard. Using a keyboard, tone combinations are generated:

- by connecting one of the row inputs to one of the column inputs by means of a single switch of the matrix
- by applying a dual contact keyboard having its common row contact tied to VN1 and the common column contact tied to VR.

Single tones can be generated by connecting the column input to VR or the row input to VN1.

An anti-bounce circuit eliminates switch bounce for up to 2 ms. Two key roll-over is provided by blocking other inputs as soon as one key is pressed.

Microcomputer mode (Figs 6 to 10)

The inputs for keyboard connections can also be used for direct connection to a microcomputer. If the column inputs are interconnected and made HIGH (= VR) the row inputs are changed to another mode, allowing the circuit to be driven by 4-bit data plus an enable signal. In this mode, it is also possible to connect a separate mute enable signal on inputs COL1, 2 and 4 and a tone enable input on COL3.

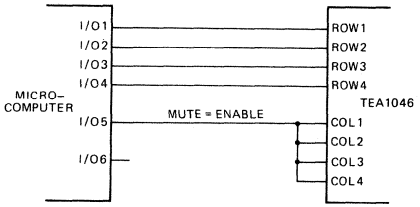


Fig. 6 Microcomputer mode.
All column inputs interconnected.

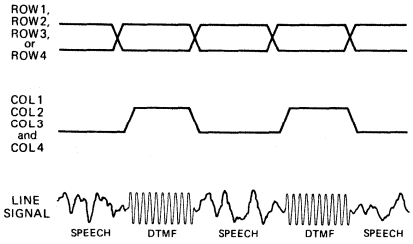


Fig. 7 Tone/speech waveform in circuit diagram Fig. 6.

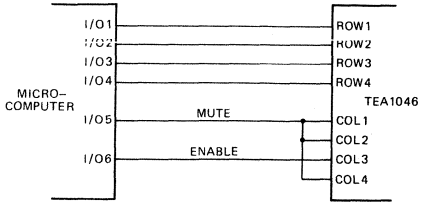
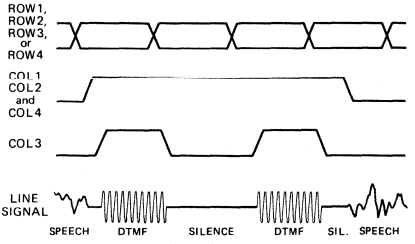


Fig. 8 Microcomputer mode.
Column inputs COL1, 2 and 4 interconnected.



7Z91000.A

Fig. 9 Tone/speech waveform in circuit diagram Fig. 8.

Truth table microcomputer mode

row				column		tones Hz	symbol	mute
1	2	3	4	1, 2, 4	3			
H	H	H	H	L	L	–	–	off
X	X	X	X	H	L	–	–	on
H	H	H	H	H	H	697/1209	1	on
H	H	H	L	H	H	697/1336	2	on
H	H	L	H	H	H	697/1477	3	on
H	H	L	L	H	H	697/1633	A	on
H	L	H	H	H	H	770/1209	4	on
H	L	H	L	H	H	770/1336	5	on
H	L	L	H	H	H	770/1477	6	on
H	L	L	L	H	H	770/1633	B	on
L	H	H	H	H	H	852/1209	7	on
L	H	H	L	H	H	852/1336	8	on
L	H	L	H	H	H	852/1477	9	on
L	H	L	L	H	H	852/1633	C	on
L	L	H	H	H	H	941/1209	*	on
L	L	H	L	H	H	941/1336	0	on
L	L	L	H	H	H	941/1477	#	on
L	L	L	L	H	H	941/1633	D	on

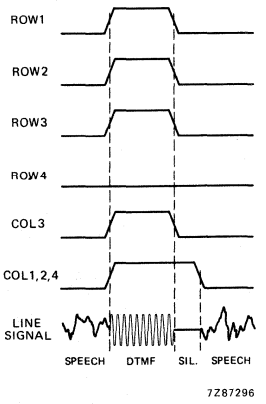


Fig. 10 Waveform tones 697/1336 Hz (dialling number 2).

Dial tone generator

The crystal oscillator frequency (3,579 545 MHz) is divided by a factor of nine to give the clock frequency. A maximum division error of 0,25% is achieved in the TEA1046; CCITT recommendations are that tones should be within 1,5% of the specified frequencies.

The output from the dividers for the higher and the lower frequency tones are symmetrical square-wave pulses which contain considerable odd-numbered harmonics. The lower order odd numbered harmonics (11th and less) are eliminated by synthesising the tone frequencies as crude stepped sinewave approximations. Each half cycle of the tone waveform comprises seven discrete amplitudes for the lower frequency tones and nine discrete amplitudes for the higher frequency tones. Each amplitude increment is generated by switching on and off an individual current source for the duration of each step of the sinewave. The frequency of the tones is varied by changing the duration of each step. This circuit allows the connecting of two low-pass first order filters to pins 9 and 10 to reduce distortion of the DTMF harmonics.

The second filter is also used for filtering the microphone signal. If lower requirements for the distortion can be applied the filter at pin 10 can be omitted. In that case the filter at pin 9 must have a lower cut-off frequency (1800 Hz) to achieve a correct pre-emphasis since the roll-off of the filters is compensated internally.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current	I_P	max.	150 mA
Surge current ($t_p < 250\ \mu s$)	I_S	max.	850 mA
Operating ambient temperature range	T_{amb}	−25 to	+70 °C
Storage temperature range	T_{stg}	−55 to	+125 °C
Junction temperature	T_j	max.	125 °C

CHARACTERISTICS

T_{amb} = 25 °C; I_L = 15 mA; f = 1 kHz; unless otherwise specified. See also Fig. 11.

parameter	symbol	min.	typ.	max.	unit
Supply					
Line voltage d.c.					
I_L = 15 mA	V_L	4,3	4,8	5,3	V
I_L = 50 mA	V_L	4,5	5,0	5,5	V
I_L = 120 mA	V_L	5,0	5,4	6,5	V
Temperature coefficient	TC	–	−10	–	mV/K
Line current range	I_L	10	–	120	mA
Stabilized voltage (pin 3)					
I_L = 15 mA	V_S	–	3,4	–	V
I_L = 120 mA	V_S	–	4,0	–	V
Reference voltage (pin 12)	V_R	–	1,0	–	V

parameter	symbol	min.	typ.	max.	unit
Microphone					
Input resistance (symmetrical)	R_i 13-14	–	4	–	kΩ
Input resistance (asymmetrical)	R_i 13	–	22	–	kΩ
Voltage amplification R_L = 600 Ω	A_M	49	50	51	dB
Temperature coefficient	TC	–	0,01	–	dB/K
Common mode rejection ratio	CMRR	60	–	–	dB
Distortion at V_L = 3 dBm	d_t	–	–	2	%
Noise output voltage Z_L = 600 Ω; psophometrically weighted (P53 curve)	V_{NO}	–	–	−65	dBmp
Amplification reduction during dialling	ΔA_M	70	–	–	dB
Anti-sidetone					
Voltage amplification, microphone to anti-sidetone output (R_{AT} = 3,9 kΩ)	A_{AT}	–	25	–	dB
Transmitter output stage					
Dynamic resistance setting range	R_i	600	–	900	Ω
Variation of output impedance over line current range R_i = 600 Ω	ΔZ_o	–	100	–	Ω
Balance return loss from 300 up to 3400 Hz at 600 Ω (R_{ZI} = 75 Ω, C_L = 10 nF)	BRL	20	–	–	dB
at 900 Ω (R_{ZI} = 120 Ω, C_L = 30 nF)	BRL	20	–	–	dB
Receiver amplifier					
Voltage amplification R_T = 350 Ω	A_T	19	20	21	dB
Amplification variation f = 300 to 3400 Hz	$\Delta A_T/f$	–	0	–	dB
Amplification variation in temperature and current range	$\Delta A_T/T$	–	–	−0,5	dB
Amplification reduction during dialling	ΔA_T	60	–	–	dB
Output voltage swing (d_t = 10%)	$V_{o(p\text{-}p)}$	1300	1600	–	mV
Output impedance	Z_o	–	4	7	Ω
Input impedance	Z_i	–	100	–	kΩ
Output distortion level < −7 dBV	d_o	–	–	2	%
Output noise voltage psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	–	150	μV
Bias current	I_M	–	3,9	–	mA

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
DTMF generator					
Tone frequencies					
low tones (row inputs)			697, 770, 852, 941		Hz
high tones (column inputs)			1209, 1336, 1477, 1633		Hz
Dividing error					
crystal frequency = 3,58 MHz	Δf_d	−0,25	–	−0,05	%
Tone output level					
$I_L > 10$ mA					
lower tones	V_{LG}	−11	–	−6	dBm
higher tones	V_{HG}	−9	–	−4	dBm
Distortion with respect to total level	d_{tot}	–	−34	−25	dB
Tolerance on output level					
over temp. and current range	ΔV_o	−2	–	2	dB
Pre-emphasis higher tones					
over temp. and current range					
at $C_{F1} = C_{F2} = 10$ nF	ΔV_{HG}	1	2	3	dB
Tone delay					
after key actuation	t_d	–	10	–	μs
Switch delay time speech/mute					
after key release	t_d	–	10	–	μs
Switch bounce elimination	t_{sb}	–	2	–	ms
Keyboard inputs					
Contact off resistance	R_{Koff}	250	–	–	kΩ
Contact on resistance	R_{Kon}	–	–	10	kΩ
Lower frequency inputs (ROW1, 2, 3, 4)					
voltage LOW	V_{IL}	–	–	1,1	V
voltage HIGH	V_{IH}	1,5	–	–	V
current LOW	I_{IL}	–	20	–	μA
current HIGH (maximum allowable = 1 mA)	I_{IH}	0	–	–	μA
Higher frequency inputs (COL1, 2, 3, 4)					
voltage LOW	V_{IL}	–	–	0,5	V
voltage HIGH	V_{IH}	0,9	–	–	V
current LOW	I_{IL}	0	–	–	μA
current HIGH (maximum allowable = 1 mA)	I_{IH}	–	20	–	μA

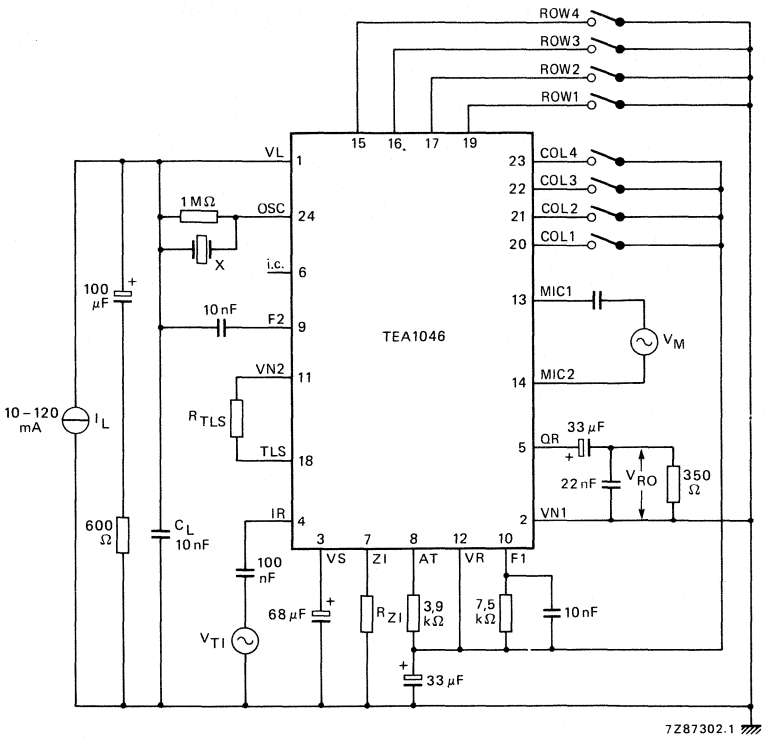


Fig. 11 Test circuit for measuring amplifier voltage gains and frequencies and levels of DTMF generator. X = 3,58 MHz.

$$A_M = \left| \frac{V_L}{V_M} \right| (V_{TI} = 0) \qquad A_T = \left| \frac{V_{RO}}{V_{IR}} \right| (V_M = 0) \qquad A_{AT} = \left| \frac{V_{AT}}{V_M} \right| (V_{TI} = 0)$$

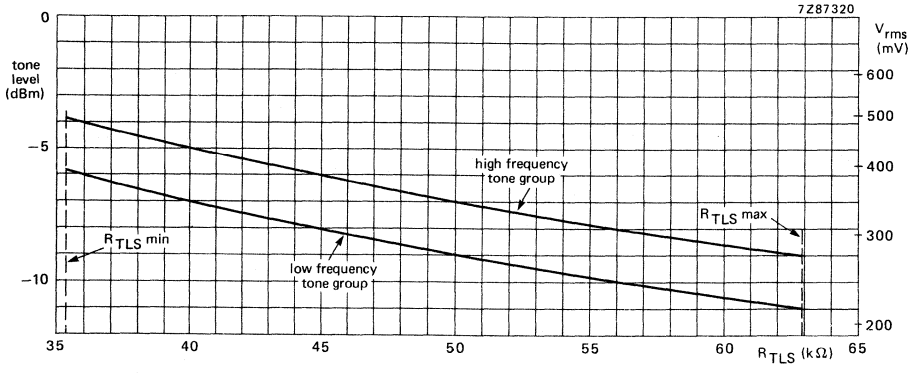


Fig. 12 DTMF level selection. The curve is valid for a dynamic impedance of 600 Ω (R_{ZI} = 75 Ω).

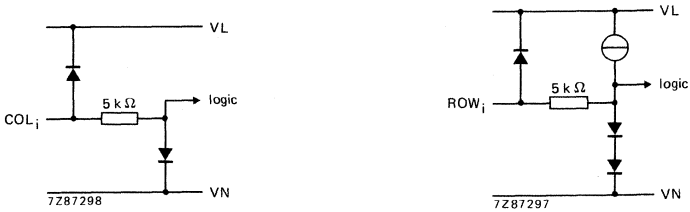


Fig. 13 Equivalent configuration of inputs: (a) COL1, 2, 3 and 4; (b) ROW1, 2, 3 and 4.

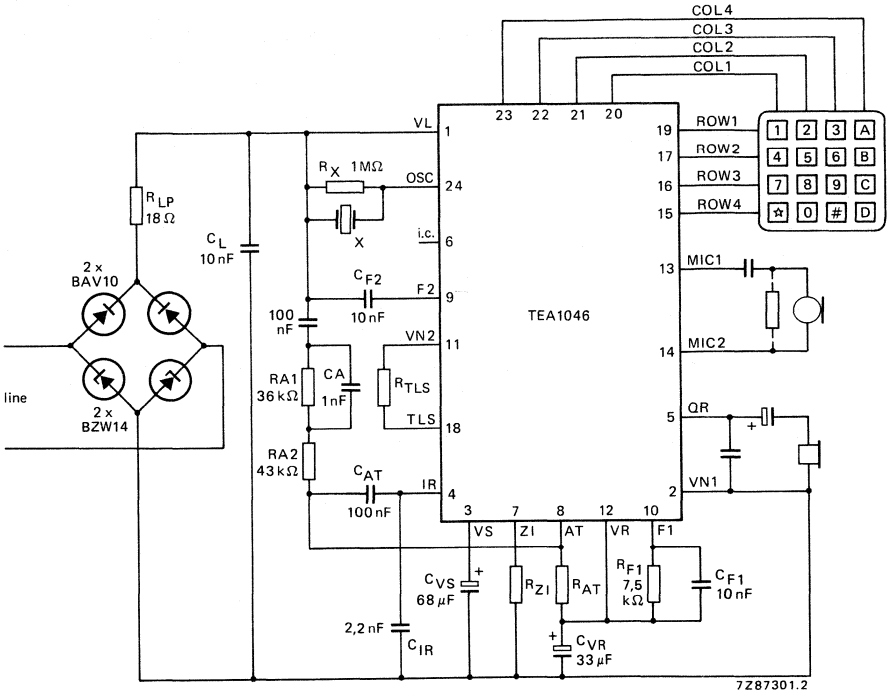


Fig. 14 Application diagram TEA1046 using dynamic transducers, R_{MS}, R_{AT}, R_{ZI} and R_{TLS} determined by transducers and system requirements.

VERSATILE TELEPHONE TRANSMISSION CIRCUITS WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1060 and TEA1061 are bipolar integrated circuits performing all speech and line interface functions required in fully electronic telephone sets. The circuits internally perform electronic switching between dialling and speech.

Features

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical low-impedance inputs for dynamic and magnetic microphones (TEA1060)
- Symmetrical high-impedance inputs for piezoelectric microphone (TEA1061)
- Asymmetrical high-impedance input for electret microphone (TEA1061)
- DTMF signal input
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large amplification setting range on all amplifiers
- Line loss compensation facility, line current dependent
- Gain control adaptable to exchange supply

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{LN}	typ.		4,35	V
Line current operating range	I_{line}	10	to	140	mA
Supply current					
power down input LOW	I_{CC}	typ.		1	mA
power down input HIGH	I_{CC}	typ.		50	μA
Voltage amplification range microphone amplifier					
TEA1060	A_{vd}	44	to	60	dB
TEA1061	A_{vd}	30	to	46	dB
receiving amplifier	A_{vd}	17	to	39	dB
Amplification control range	ΔA_{vd}	typ.		6	dB
Exchange supply voltage range	V_{exch}	24	to	60	V
Exchange feeding bridge resistance range	R_{exch}	400	to	1000	Ω
Operating ambient temperature range	T_{amb}	−25	to	+75	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102A).

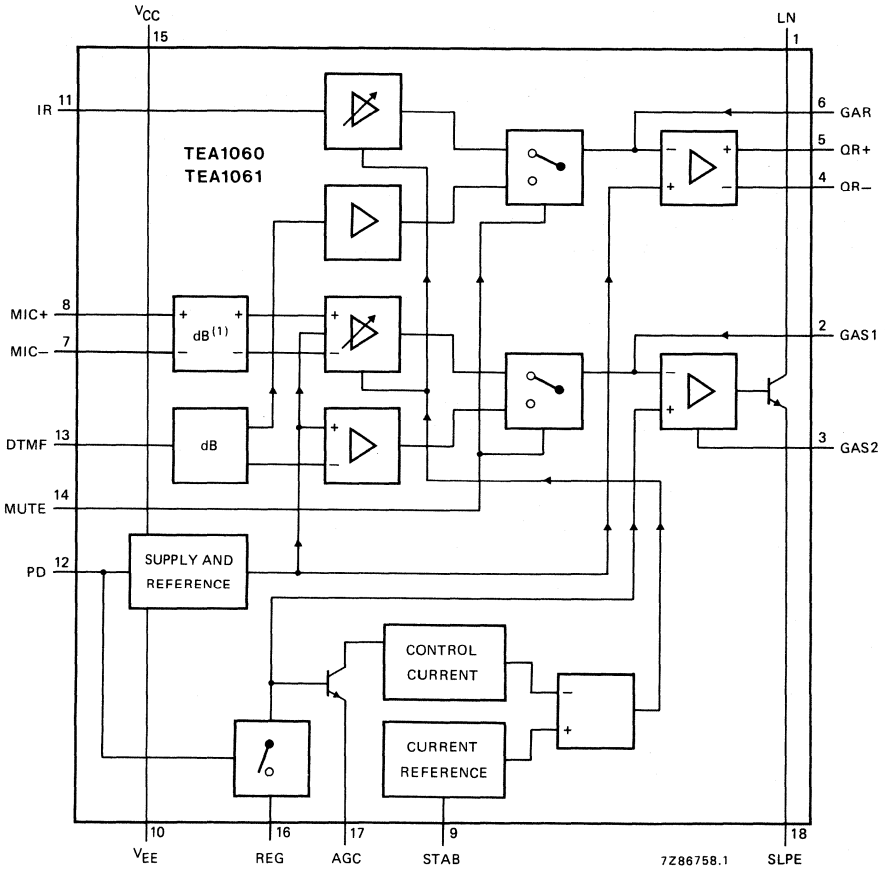


Fig. 1 Block diagram. The blocks marked "dB" are attenuators. The block marked (1) is only present in the TEA1061.

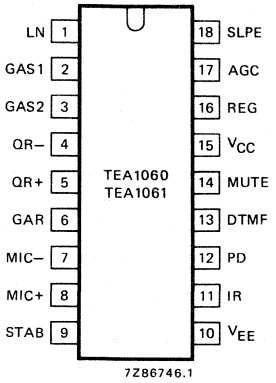


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (d.c. resistance) adjustment

DEVELOPMENT SAMPLE DATA

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripheral circuits usually are supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3,6 kΩ between STAB and V_{EE}.

The d.c. current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the d.c. resistance of the subscriber line R_{line} and the d.c. voltage on the subscriber set (see Fig. 3).

If the line current I_{line} exceeds the current I_{CC} + 0,5 mA required by the circuit itself ($I_{CC} \approx 1$ mA), plus the current I_p required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0{,}5.10^{-3} - I_P) \times R9.$$

V_{ref} being an internally generated temperature compensated reference voltage of 4,1 V and R9 being an external resistor connected between SLPE and V_{EE}. Under normal conditions $I_{SLPE} \gg I_{CC} + 0{,}5$ mA + I_P. The static behaviour of the circuit then equals a 4,1 V voltage regulator diode with an internal resistance R9. In the audio-frequency range the dynamic impedance equals R1.

FUNCTIONAL DESCRIPTION (continued)

The current I_p available from V_{CC} for supplying peripheral circuits depends on external components, and on the line current. Figure 4 shows this current for V_{CC} = 3 V min., this being the minimum supply voltage for most CMOS circuits including a diode voltage drop for an enable diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven.

Microphone inputs MIC+ and MIC− and gain adjustment pins GAS1 and GAS2

The TEA1060 and TEA1061 have symmetrical microphone inputs.

The TEA1060 is intended for low-sensitivity, low-impedance dynamic or magnetic microphones. Its input impedance is 2 x 4 kΩ and its voltage amplification is typ. 52 dB.

The TEA1061 is intended for a piezoelectric microphone or an electret microphone with built-in FET source follower. Its input impedance is 2 x 20 kΩ and its voltage amplification is typ. 38 dB.

The arrangements with the microphone types mentioned are shown in Fig. 5.

The amplification of the microphone amplifier in both types can be adjusted over a range of ± 8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Mute input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier, a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage amplification from DTMF to LN is typ. 26 dB and varies with R7 in the same way as the amplification of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR−. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig. 6). Amplification from IR to QR+ is typ. 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the amplification is increased by 6 dB. This makes differential drive possible, which is required for high-impedance dynamic, magnetic and piezoelectric earpieces with load impedances exceeding 450 Ω.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and r.m.s. value is higher.

The amplification of the receiving amplifier can be adjusted over a range of ± 8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R4 connected from GAR to QR+.

Two external capacitors C4 = 100 pF and C7 = 10 x C4 = 1 nF are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order, low-pass filter. The "cut-off" frequency corresponds with the time constant R4 x C4.

Automatic gain control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the amplification of the microphone amplifier and the receiving amplifier in accordance with the d.c. line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0,5 mm diameter copper twisted-pair cable with a d.c. resistance of 176 Ω/km and an average attenuation of 1,2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 7 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range.

If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum amplification as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input, which reduces the supply current from typ. 1 mA to typ. 50 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the circuit's impedance equals a 4,1 V voltage regulator diode with an internal resistance equal to R9. This results in rectangular current waveforms in pulse dialling and register recall.

When this facility is not required PD may be left open.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of R2, R3, R8 and Z_{bal} (see Fig. 10). Maximum compensation is obtained when Z_{bal}/k equals the line impedance Z_{line} as seen by the set (scale factor $k = R_8/R_1$).

In practice Z_{line} varies strongly with line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal}/k equals the average line impedance.

The anti-side-tone network attenuates the signal from the line. With R8 = 390 Ω and R9 = 20 Ω the attenuation is 32 dB. The attenuation is nearly flat over the audio-frequency range.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Positive line voltage	V_{LN}	max.	13,2	V
Line current				
average	$I_{line(AV)}$	max.	140	mA
non-repetitive (t_{max} = 100 hours)	$I_{line(S)}$	max.	250	mA
non-repetitive peak (t_{max} = 1 ms)	$I_{line(SM)}$	max.	1	A
Voltage on all other pins	V	max.	V_{CC} + 0,7	V
	−V	max.	0,7	V
Total power dissipation	P_{tot}	max.	640	mW
Storage temperature range	T_{stg}	−40 to	+125	°C
Operating ambient temperature range	T_{amb}	−25 to	+75	°C

CHARACTERISTICS

I_{line} = 10 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 15)					
Voltage drop over circuit					
at I_{line} = 5 mA	V_{LN}	–	4,15	–	V
at I_{line} = 15 mA	V_{LN}	4,15	4,35	4,55	V
at I_{line} = 100 mA	V_{LN}	–	6,0	7	V
Variation with temperature at I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	−4	−2	0	mV/K
Supply current					
at V_{CC} = 2,8 V; PD = LOW	I_{CC}	–	0,96	1,25	mA
at V_{CC} = 2,8 V; PD = HIGH	I_{CC}	–	50	–	μA
Microphone inputs MIC+ and MIC−					
Input impedance					
TEA1060	$\lvert z_{is} \rvert$	–	4	–	kΩ
TEA1061	$\lvert z_{is} \rvert$	–	20	–	kΩ
Standard deviation on input impedance	σ	–	12	–	%
Common-mode rejection ratio; TEA1060	k_{CMR}	–	80	–	dB
Voltage amplification at I_{line} = 15 mA; R7 = 68 kΩ					
TEA1060	A_{vd}	51	52	53	dB
TEA1061	A_{vd}	37	38	39	dB
Variation with frequency at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	–	±0,2	–	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to +75 °C	$\Delta A_{vd}/\Delta T$	–	±0,5	–	dB

parameter	symbol	min.	typ.	max.	unit
Dual-tone multi-frequency input DTMF					
Input impedance	$\|z_{is}\|$	–	20	–	kΩ
Standard deviation on input impedance	σ	–	12	–	%
Voltage amplification at I_{line} = 15 mA; R7 = 68 kΩ	A_{vd}	25	26	27	dB
Variation with frequency at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	–	±0,2	–	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to +75 °C	$\Delta A_{vd}/\Delta T$	–	±0,5	–	dB
Gain adjustment pins GAS1 and GAS2					
Amplification variation with R7, transmitting amplifier	ΔA_{vd}	−8	–	+8	dB
Transmitting amplifier output LN					
Output voltage at I_{line} = 15 mA; d_{tot} = 2%	$V_{LN(rms)}$	1,4	2,3	–	V
d_{tot} = 10%	$V_{LN(rms)}$	–	2,6	–	V
Noise output voltage at I_{line} = 15 mA; R7 = 68 kΩ; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	−70	–	dBmp
Receiving amplifier input IR					
Input impedance	$\|z_{is}\|$	–	20	–	kΩ
Receiving amplifier outputs QR+ and QR−					
Output impedance; single-ended	$\|z_{os}\|$	–	4	–	Ω
Voltage amplification at I_{line} = 15 mA; R4 = 100 kΩ; single-ended; R_L = 300 Ω	A_{vd}	24	25	26	dB
differential; R_L = 600 Ω	A_{vd}	30	31	32	dB
Variation with frequency, at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	–	±0,2	–	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to +75 °C	$\Delta A_{vd}/\Delta T$	–	±0,5	–	dB
Output voltage at I_p = 0; d_{tot} = 2%; sine-wave drive single-ended; R_L = 150 Ω	$V_{o(rms)}$	0,3	0,38	–	V
single-ended; R_L = 450 Ω	$V_{o(rms)}$	0,4	0,52	–	V
differential; C_L = 47 nF + R_L = 100 Ω; f = 3400 Hz	$V_{o(rms)}$	0,8	1,0	–	V
Noise output voltage at I_{line} = 15 mA; R4 = 100 kΩ; psophometrically weighted (P53 curve) single-ended; R_L = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential; R_L = 600 Ω	$V_{no(rms)}$	–	100	–	μV

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Gain adjustment pin GAR					
Amplification variation with R4, receiving amplifier	ΔA_{vd}	−8	–	+8	dB
MUTE input					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	V_{IL}	–	–	0,3	V
Input current	I_{MUTE}	–	8	15	μA
Reduction of voltage amplification from MIC+ and MIC− to LN at MUTE = HIGH	$-\Delta A_{vd}$	–	70	–	dB
Voltage amplification from DTMF to QR + or QR− at MUTE = HIGH; single-ended load; R_L = 300 Ω	A_{vd}	–	−18	–	dB
Power-down input PD					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	V_{IL}	–	–	0,3	V
Input current	I_{PD}	–	5	10	μA
Automatic gain control input AGC					
Amplification control range	$-\Delta A_{vd}$	–	6	–	dB
Highest line current for maximum amplification at R6 = 110 kΩ	I_{line}	–	22	–	mA
Lowest line current for minimum amplification at R6 = 110 kΩ	I_{line}	–	60	–	mA

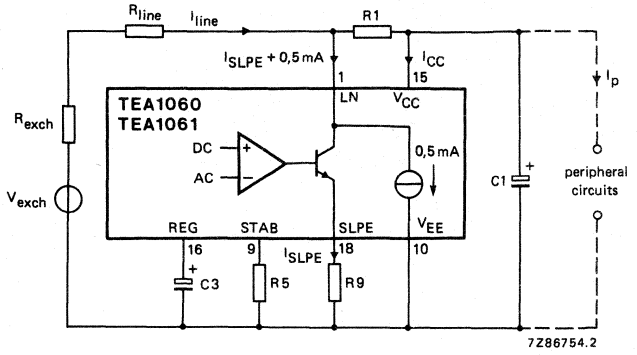


Fig. 3 Supply arrangement.

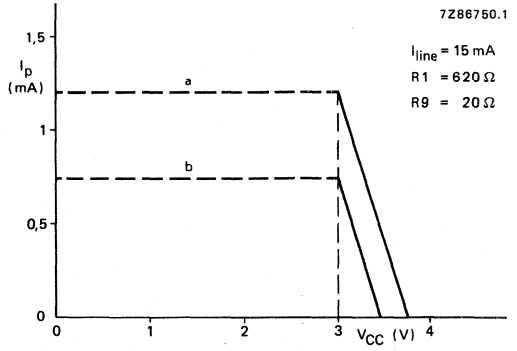


Fig. 4 Maximum current I_p available from V_{CC} for external (peripheral) circuitry with $V_{CC} \geqslant 3$ V. Curve "a" is valid when the receiving amplifier is not driven or when MUTE = HIGH, curve "b" is valid when MUTE = LOW and the receiving amplifier is driven, $V_{o(rms)} = 150$ mV, $R_L = 150\ \Omega$.

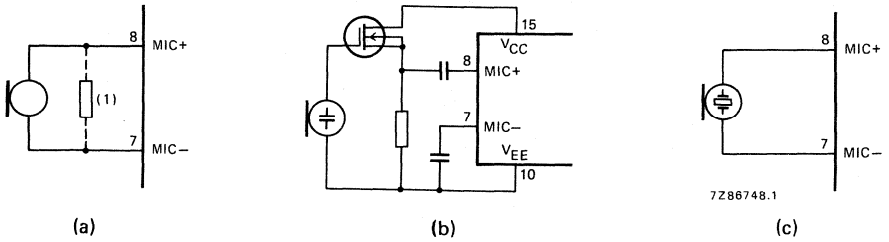


Fig. 5 Alternative microphone arrangements. (a) magnetic or dynamic microphone, TEA1060. The resistor marked (1) may be connected to lower the terminating impedance. (b) electret microphone, TEA1061. (c) piezoelectric microphone, TEA1061.

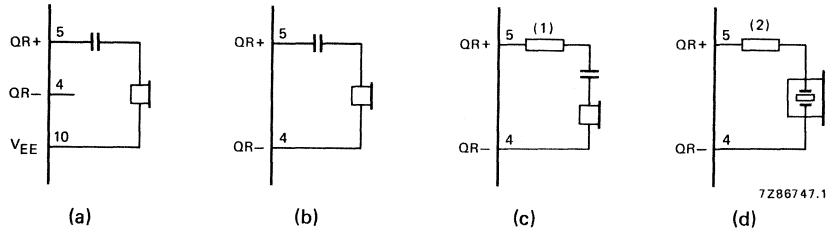


Fig. 6 Alternative receiver arrangements. (a) dynamic telephone with less than 450 Ω impedance. (b) dynamic telephone with more than 450 Ω impedance. (c) magnetic telephone with more than 450 Ω impedance. The resistor marked (1) may be connected to obtain an appropriate acoustic frequency characteristic. (d) piezoelectric telephone. The resistor marked (2) is required to increase the phase margin.

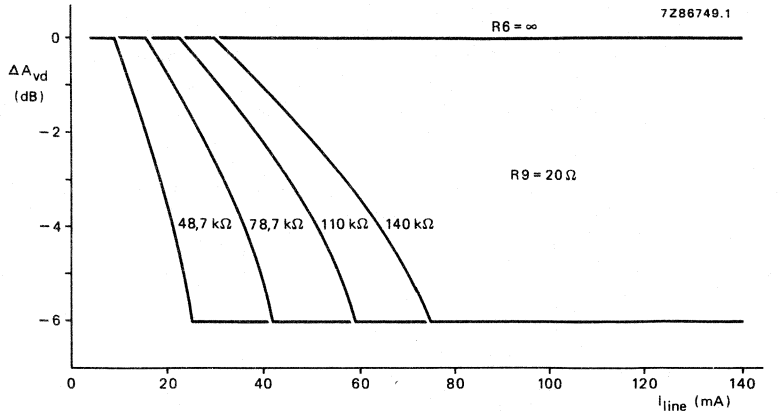


Fig. 7 Variation of amplification with line current, with R6 as a parameter.

Table 1. Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	24	61,9	48,7	X	X
	36	100	78,7	68	60,4
	48	140	110	93,1	82
	60	X	X	120	102

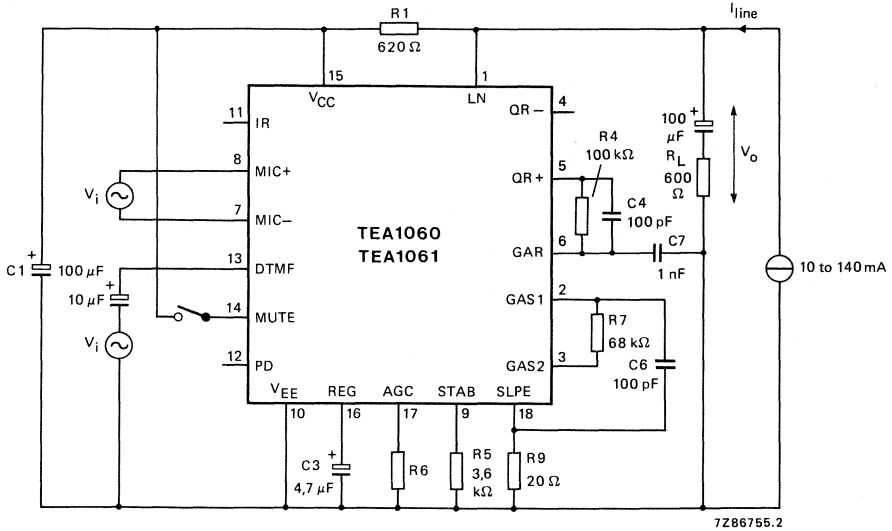


Fig. 8 Test circuit for defining voltage amplification of MIC+, MIC– and DTMF inputs. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$. For measuring the amplification from MIC+ and MIC– the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

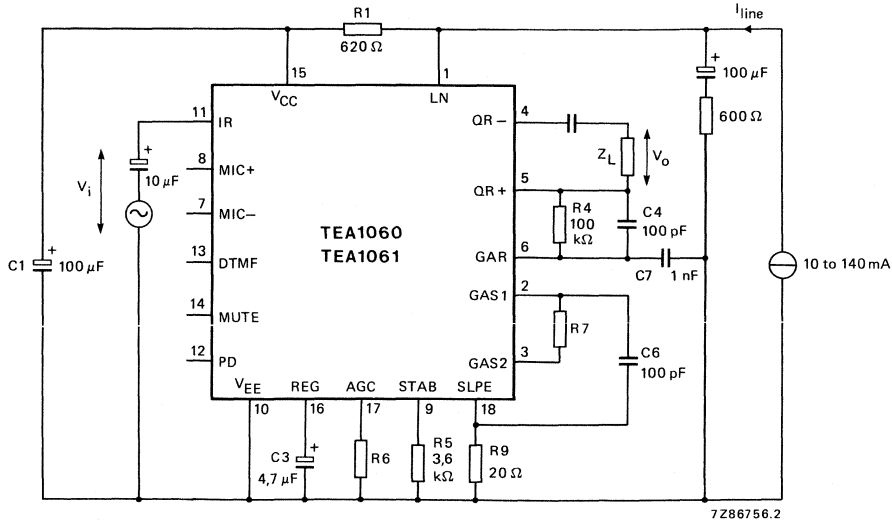


Fig. 9 Test circuit for defining voltage amplification of the receiving amplifier. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

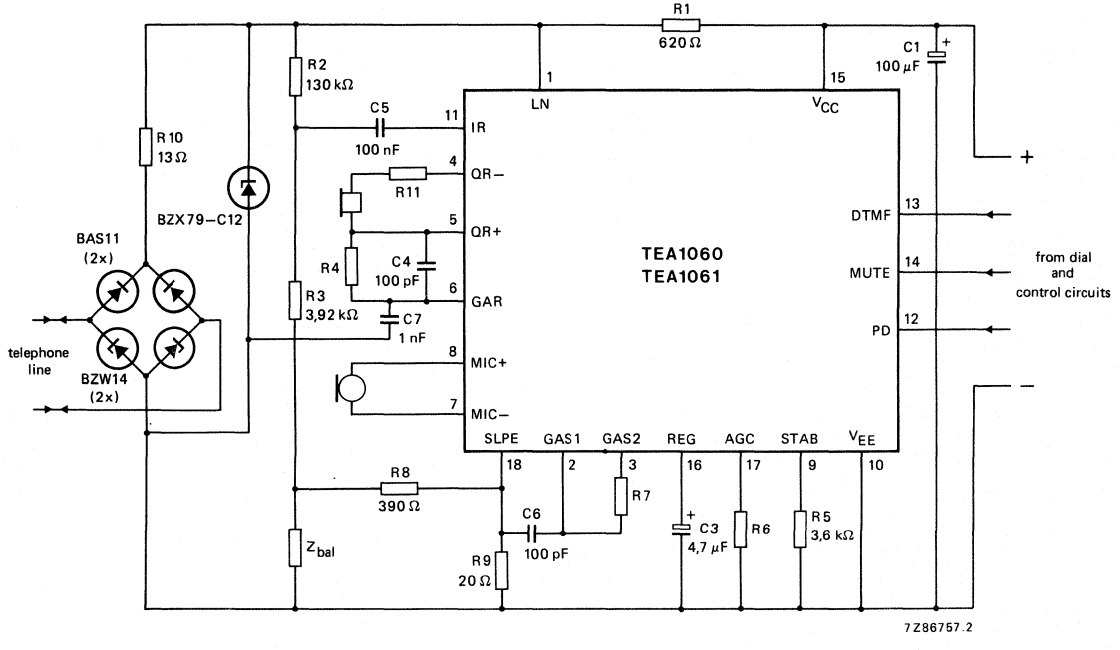


Fig. 10 Typical application of the TEA1060 or TEA1061, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left, the zener diode and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

APPLICATION INFORMATION SUPPLIED ON REQUEST

APPLICATION INFORMATION (continued)

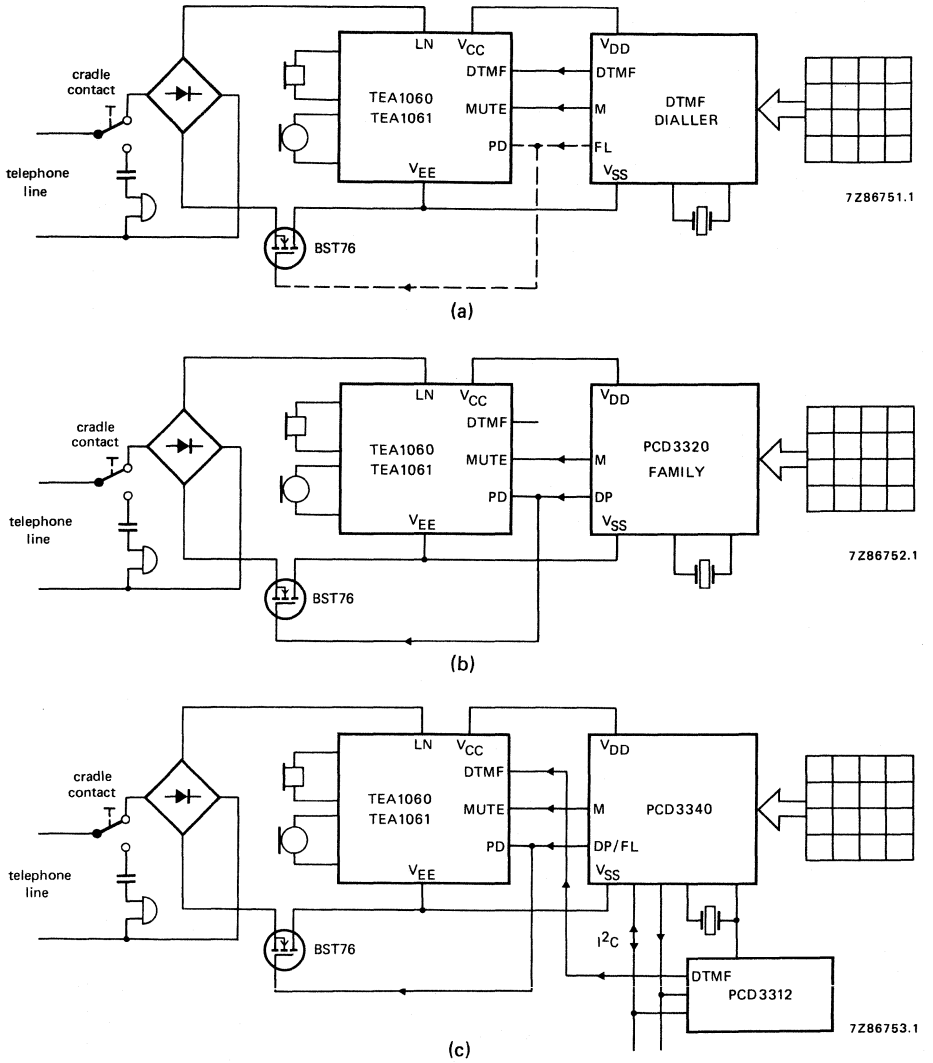


Fig. 11 Typical applications of the TEA1060 or TEA1061 (simplified).

(a) DTMF set with a CMOS DTMF dialling circuit. The dashed lines show an optional flash (register recall by timed loop break).
(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.
(c) Dual-standard (pulse and DTMF) feature phone with the PCD3340 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C bus.

DTMF GENERATOR FOR TELEPHONE DIALLING

This integrated circuit is a dual tone multi-frequency (DTMF) generator with line interface for use in push button telephone sets containing an electronic speech circuit or a conventional hybrid transformer. The IC contains a mute switch handling the full line current, which allows two-wire connection between dial and speech parts. The logic inputs can be operated with a single contact keyboard or via a direct interface with a microcomputer. I^2L technology allows digital and analogue functions to be implemented on the same chip. The line interface incorporates a filter amplifier, an output stage and a voltage stabilizer all of which are switched off when the speech circuit is connected to the line. The tone generator is supplied by a temperature compensated current stabilizer and is be driven by a 3,58 MHz crystal.

The logic inputs contain an interface circuit to guarantee well-defined states of the keyboard.

Features:

- two wire connection between dial and speech parts allowed
- wide operating line current and temperature range
- operating voltage down to 1,7 V
- no individual tone level adjustment required
- few external components required
- all mute functions on chip
- common inputs for keyboard and microcomputer
- temperature and line current independent signal levels
- all pins protected against electrostatic discharges
- on-chip output stage and line regulator
- single tone generation possibility

QUICK REFERENCE DATA

Operating voltage	V_L	typ. 3,3	V
Line current range	I_L	10 to 120	mA
DTMF levels (adjustable)			
low frequency	V_{LG}	−11 to −6	dBm
high frequency	V_{HG}	−9 to −4	dBm
Pre-emphasis	$V_{HG}-V_{LG}$	max. 2	dB
Operating temperature range	T_{amb}	−25 to +70	°C

PACKAGE OUTLINE

TEA1075P: 18-lead DIL, plastic (SOT-102HE).

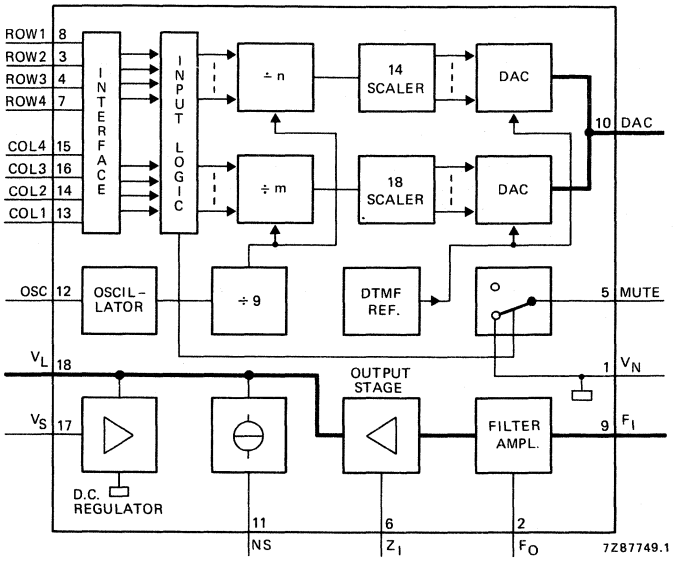


Fig. 1 Functional block diagram.

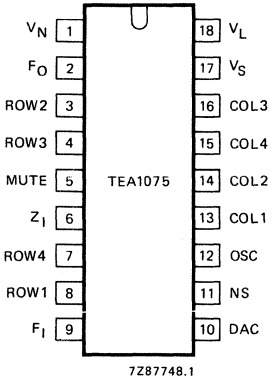


Fig. 2 Pin designation.

PINNING

1	V_N	negative line voltage
2	F_O	filter output
3	ROW2	row input 770 Hz/BCD input
4	ROW3	row input 852 Hz/BCD input
5	MUTE	mute switch
6	Z_I	impedance setting terminal
7	ROW4	row input 941 Hz/BCD input
8	ROW1	row input 697 Hz/BCD input
9	F_I	filter input
10	DAC	DTMF level setting
11	NS	noise suppression input
12	OSC	oscillator input
13	COL1	column input 1209 Hz/mute input
14	COL2	column input 1336 Hz/mute input
15	COL4	column input 1633 Hz/mute input
16	COL3	column input 1477 Hz/enable input
17	V_S	voltage stabilizer filter
18	V_L	positive line voltage

FUNCTIONAL DESCRIPTION

Voltage regulator

The voltage regulator switches on as a keyboard button is pressed. It regulates the voltage drop across the IC to a nominal level of 3,3 V, shunting excess line current to maintain a working current of 8 mA within the chip. The voltage regulator is switching to a higher voltage level when the keyboard switch is released.

The capacitor connected to input V_S provides a low-pass filter function to avoid influence of audio signals on the line. For a short period during switch-on time the capacitor is directly connected to the line to reduce overshoot voltages to only 1 V above the voltage set by the regulator.

In order to adapt the nominal d.c. level to the level as set by the speech circuit, a resistor can be connected either between V_L and V_S or between V_N and V_S. This will decrease or increase the level respectively. During the time the device is in the stand-by mode the voltage stabilizer circuit will conduct again as the d.c. line voltage set by the speech part achieves 6,0 V. Part of the line current then will flow through this stabilizer.

Active output stage

The transmitter amplifier consists of a voltage to current convertor with a class-A output stage. The circuit acts as a dynamic resistance (R_a) because of the feedback from the line to the input. This impedance can be set by output Z_I at pin 6:
R_a = 900 Ω if pin 6 is left open
R_a = 600 Ω if pin 6 is connected to V_N (pin 1).
The impedance is extremely high as long as no key is depressed (stand-by mode).

Speech muting

Figure 3 shows the connection of the dial circuit with a speech circuit TEA1060/61. All mute functions are performed by internal switches. Pressing any keyboard push button switches the TEA1075 to operating mode and isolates the speech circuit from the line.

The line adaption then is taken over by the dial circuit which causes:
- line voltage to be set by the voltage regulator TEA1075
- impedance to be set by the active output stage TEA1075
- audio output stage to be connected to the line for DTMF tone transmission.

During the stand-by mode (no key pressed) the voltage on the line is set by the speech circuit. The minimum d.c. operating voltage of the dial circuit for guaranteed detection of push button operation on the keyboard is 2,5 V. The impedance is approximately 10 kΩ and the current consumption 2 mA. The stand-by current is used for the logic part as well as driving current for the internal mute switch which can switch the full line current available.

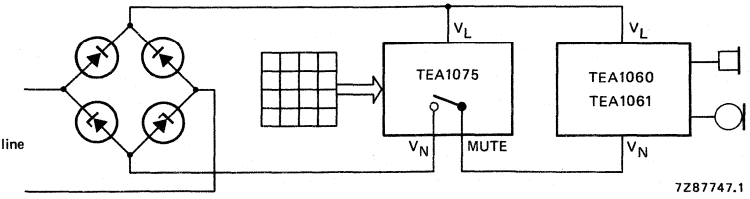


Fig. 3 Muting system.

FUNCTIONAL DESCRIPTION (continued)

OSC and DTMF generator

The crystal oscillator frequency (3,579 545 MHz) is divided by a factor of nine to give the clock frequency. A maximum division error of 0,31% is achieved in the TEA1075; CCITT recommendations are that tones should be within 1,5% of the specified frequencies.
A bias resistor of 1 to 4,7 MΩ must be connected between the oscillator input and V_P. An external frequency generator can be connected instead of a crystal (see Fig. 5).

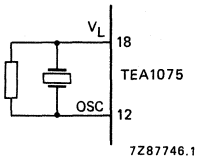


Fig. 4 Quartz crystal oscillator.

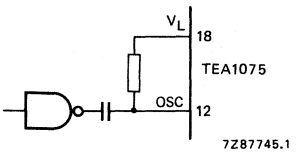


Fig. 5 External frequency generator.

The output from the dividers for the higher and the lower frequency tones are symmetrical square-wave pulses which contain considerable odd-numbered harmonics. The lower order odd-numbered harmonics (11th and less) are eliminated by synthesising the tone frequencies as crude stepped sinewave approximations. Each half cycle of the tone waveform comprises seven discrete amplitudes for the lower frequency tone and nine for the higher frequency tone. Each amplitude increment is generated by switching on and off an individual current source for the duration of each step of the sine wave. The frequency of the tones is varied by changing the duration of each step. This circuit allows the connection of a first or second order filter, depending on the distortion requirements (see filter and DTFM level).

Deviation of ROW and COLUMN frequencies

	freq. Hz	deviation %	real Hz
ROW1	697	−0,24	695,33
ROW2	770	−0,28	767,81
ROW3	852	−0,25	849,84
ROW4	941	−0,31	938,04

	freq. Hz	deviation %	real Hz
COL1	1209	−0,31	1205,23
COL2	1337	−0,10	1334,66
COL3	1477	−0,27	1473,06
COL4	1633	−0,18	1630,03

Filter and DTMF level

The output current from the DAC causes a voltage drop across R_{TLS} at pin 10. At this point the signal path is broken to allow insertion of filter components in series with the amplifier input at pin 9. The output of this amplifier is brought out to pin 2 to allow connection of filter components in the feedback path to provide additional attenuation of the higher-order odd harmonics of the tone frequencies.

The output amplitude of the tones is directly proportional to the value of R_{TLS} and can therefore be adjusted to meet specific requirements. Fig. 6 shows the output level as function of R_{TLS} and R_a = 600 Ω. If R_a = 900 Ω R_{TLS} must be devided by 1,25.

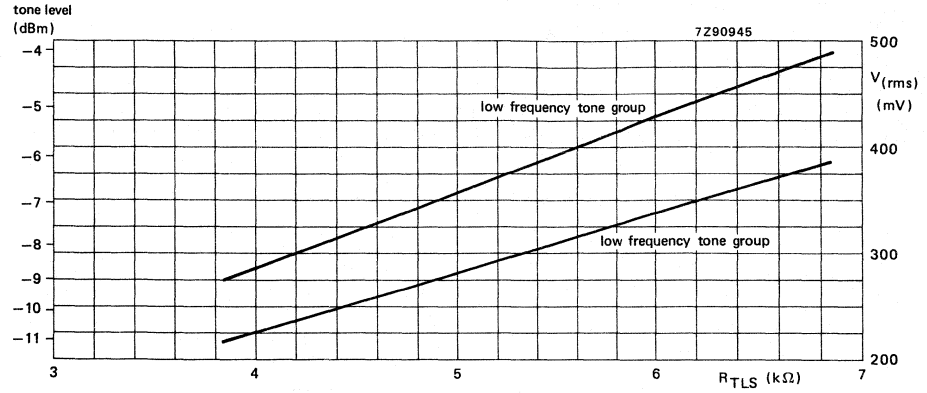


Fig. 6 DTMF level selection.

When R_{TLS} is selected for the required tone level, C_{FI} can be calculated to avoid too much influence of the filter characteristic on the pre-emphasis parameter, the time constant for a single pole filter is:

$R_{TLS} \cdot C_{FI} = 26\ \mu s$ (see Fig. 16).

If higher attenuation is required a second-order filter can be applied. The time constant for such is:

$R_{TLS} \cdot C_{FO} = R_{FS} \cdot C_{FI} = 46\ \mu s$ (see Fig. 15).

Keyboard inputs

Inputs for the logic control are compatible with different types of keyboards. Using a keyboard, tone combinations are generated:

- by connecting one of row inputs to one of the column inputs by means of a single switch of the matrix
- or by applying a dual contact keyboard having its common row contact tied to V_N and the common column contact via 68 kΩ to V_L.

Single tones can be generated by connecting a row input to V_N (pin 1) or one of the column inputs a 68 kΩ resistor to V_L (pin 18).

An anti-bounce circuit eliminates switch bounce.

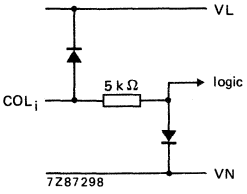


Fig. 7 Configuration of column inputs.

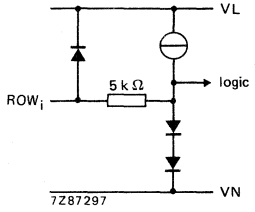


Fig. 8 Configuration of row inputs.

Microcomputer mode

The inputs for the keyboard connections can be used for direct connection to a microcomputer. If the column inputs are interconnected and made 'HIGH' (> 1 V or $I_{cd} = 30\ \mu A$) the row inputs are changed to another mode, allowing the circuit to be driven by 4-bit data plus an enable signal. In this mode, it is possible to connect a separate mute enable signal on inputs COL1, 2 and 4 and a tone enable input on COL3.

FUNCTIONAL DESCRIPTION (continued)

Truth table microcomputer mode

row				column		tones	symbol	mute *
1	2	3	4	1, 2, 4	3	Hz		
H	H	H	H	L	L	–	–	off
X	X	X	X	H	L	–	–	on
H	H	H	H	H	H	697/1209	1	on
H	H	H	L	H	H	697/1336	2	on
H	H	L	H	H	H	697/1477	3	on
H	H	L	L	H	H	697/1633	A	on
H	L	H	H	H	H	770/1209	4	on
H	L	H	L	H	H	770/1336	5	on
H	L	L	H	H	H	770/1477	6	on
H	L	L	L	H	H	770/1633	B	on
L	H	H	H	H	H	852/1209	7	on
L	H	H	L	H	H	852/1336	8	on
L	H	L	H	H	H	852/1477	9	on
L	H	L	L	H	H	852/1633	C	on
L	L	H	H	H	H	941/1209	*	on
L	L	H	L	H	H	941/1336	0	on
L	L	L	H	H	H	941/1477	#	on
L	L	L	L	H	H	941/1633	D	on

* Mute "on" = switch open.

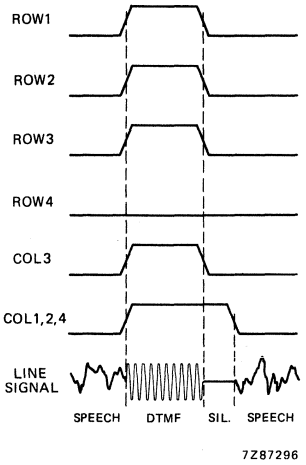


Fig. 9 Waveform tones 697/1336 Hz (dialling number 2).

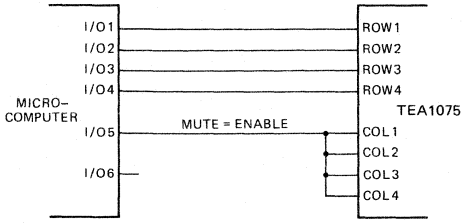


Fig. 10 Microcomputer mode.
All column inputs interconnected.

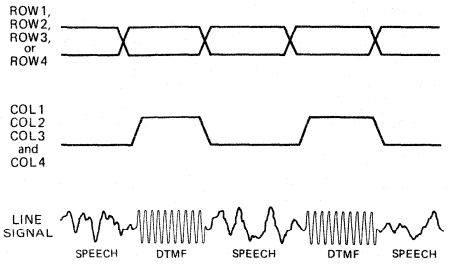


Fig. 11 Tone/speech waveform
in circuit diagram Fig. 10.

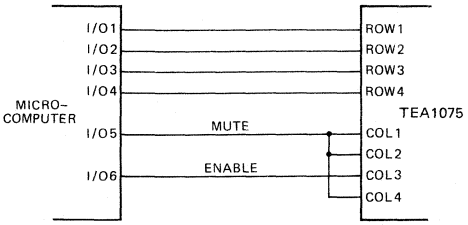


Fig. 12 Microcomputer mode.
Column inputs COL1, 2 and 4
interconnected.

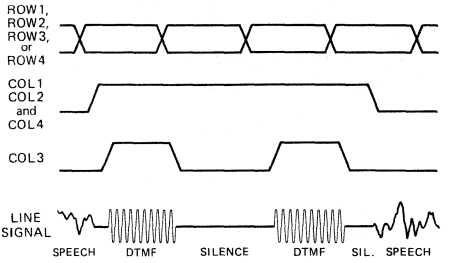


Fig. 13 Tone/speech waveform
in circuit diagram Fig. 12.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current	I_P	max.	150	mA
Surge current ($t_p < 250\ \mu s$)	I_S	max.	1000	mA
Operating ambient temperature range	T_{amb}		−25 to +70	°C
Storage temperature range	T_{stg}		−55 to +125	°C
Voltage on any pin	V_I		$(V_N-0,3)$ to $(V_L+0,3)$	V
Line voltage	V_{L-N}	max.	10	V
Power dissipation	P_{tot}	max.	750	mW

CHARACTERISTICS

T_{amb} = 25 °C; I_L = 15 mA; f = 1 kHz; unless otherwise specified. See also Fig. 14.

description	symbol	min.	typ.	max.	unit
Supply					
Line voltage d.c. (operating mode)					
I_L = 15 mA	V_L	–	3,3	–	V
I_L = 50 mA	V_L	–	3,7	–	V
I_L = 120 mA	V_L	–	4,5	–	V
Line voltage d.c. (stand-by mode)	V_L	–	–	6,5	V
Temperature coefficient	TC	–	–8	–	mV/K
Line current range	I_L	10	–	120	mA
Transmitter output stage					
Dynamic resistance setting range					
pin 6 open	R_i	–	900	–	Ω
pin 6 connected to V_N	R_i	–	600	–	Ω
Variation over line current					
R_i = 600 Ω	ΔZ_o	–	100	–	Ω
Gain	A_{TL}	–	t.b.f.	–	dB
Balance return loss from 300 up to 3400 Hz					
at 600 Ω	BRL	20	–	–	dB
at 900 Ω (C_L = 30 nF)	BRL	20	–	–	dB
Total harmonic distortion with respect to total output level (second-order filter)	d_{tot}	–	–40	–25	dB
DTMF generator					
Tone frequencies					
low tones (row inputs)			697, 770, 852, 941		Hz
high tones (column inputs)			1209, 1336, 1477, 1633		Hz
Dividing error					
crystal frequency = 3,579545 MHz	Δf_d	–0,31	–	–0,1	%
Tone output level (adjustable)					
$I_L > 10$ mA					
lower tones	V_{LG}	–11	–	–8	dBm
higher tones	V_{HG}	–9	–	–6	dBm
$I_L > 12$ mA					
lower tones	V_{LG}	–11	–	–6	dBm
higher tones	V_{HG}	–9	–	–4	dBm
Tolerance on output level over temp. and current range	ΔV_o	–2	–	2	dB
Pre-emphasis higher tones/lower tones over temp. and current range	ΔV_{HG}	1	2	3	dB
Tone delay after key actuation	t_d	–	–	5	ms
Switch bounce elimination	t_{sb}	–	2	–	ms

description	symbol	min.	typ.	max.	unit
Mute					
Mute output sink current (no key pressed)	I_{MSS}	–	–	120	mA
Saturation voltage (I_{MS} = 75 mA)	$V_{MT(sat)}$	–	150	500	mV
Maximum voltage (voltage set by speech part)	V_{MT}	–	–	10	V
Stand-by current (V_L = 4,5 V)	I_{STB}	–	2	2,5	mA
Switch delay after key release	t_d	–	–	10	μs
Resistance	R_M	–	10	–	kΩ
Keyboard inputs (microcomputer inputs)					
Contact off resistance	R_{Koff}	300	–	–	kΩ
Contact on resistance	R_{Kon}	–	–	10	kΩ
Lower frequency inputs (ROW1, 2, 3, 4)					
voltage LOW	V_{IL}	–	–	1,1	V
voltage HIGH	V_{IH}	1,5	–	–	V
current (d.c.) at V_{IL} dial mode	I_{ILD}	–	30	–	μA
Higher frequency inputs (COL1, 2, 3, 4)					
voltage LOW	V_{IL}	–	–	0,5	V
voltage HIGH	V_{IH}	0,9	–	–	V
current (d.c.) at V_{IH} dial mode	I_{IHD}	–	30	–	μA

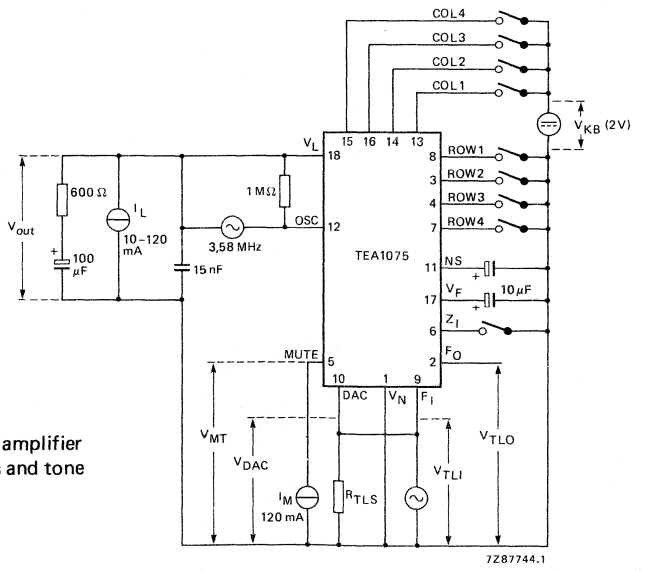


Fig. 14 Test circuit measuring amplifier voltage gain (A_{TL}) frequencies and tone output levels of the generator

$$A_{TL} = \left| \frac{V_{TLO}}{V_{TLI}} \right|$$

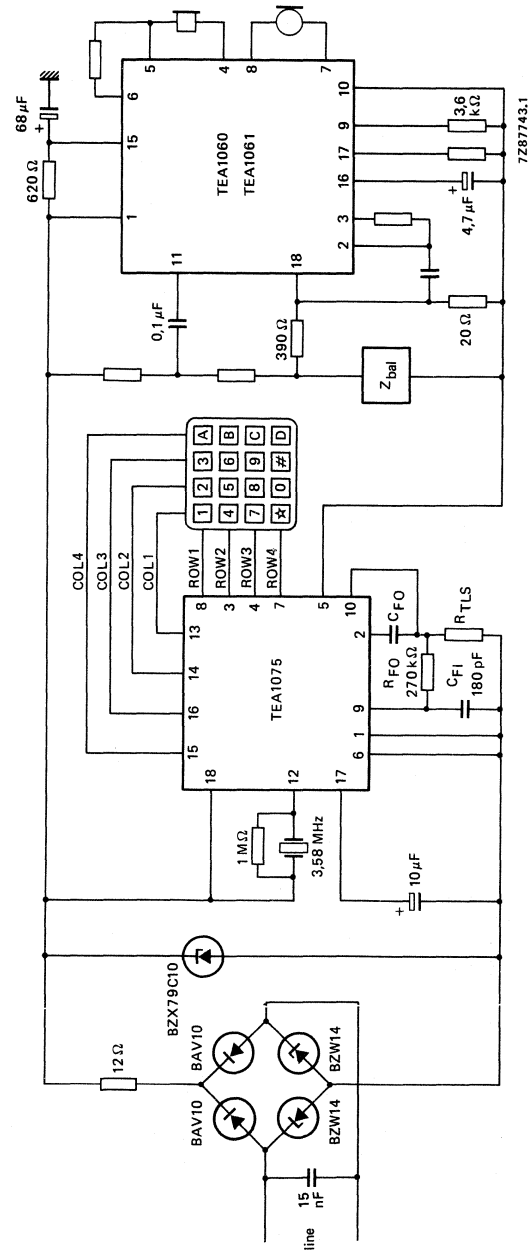


Fig. 15 Application diagram TEA1075 using a second-order filter for low harmonic distortion (CEPT T/CS 34-08). Dial and speech functions are complete separated, so line adaption is done either by TEA1075 or TEA1060. The diagram shows a complete DTMF telephone set including protection. Both circuits are set to an impedance of 600 Ω.

DEVELOPMENT SAMPLE DATA

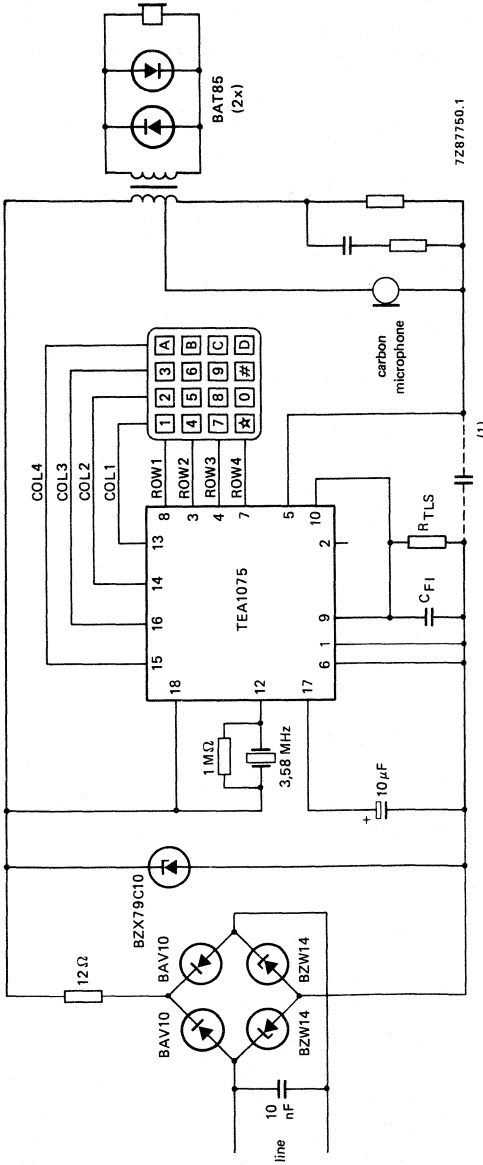


Fig. 16 Application diagram TEA1075 using a single pole filter.
The diagram shows a complete DTMF set including protection.

* C_{CT} connected only if confidence tone is desired.

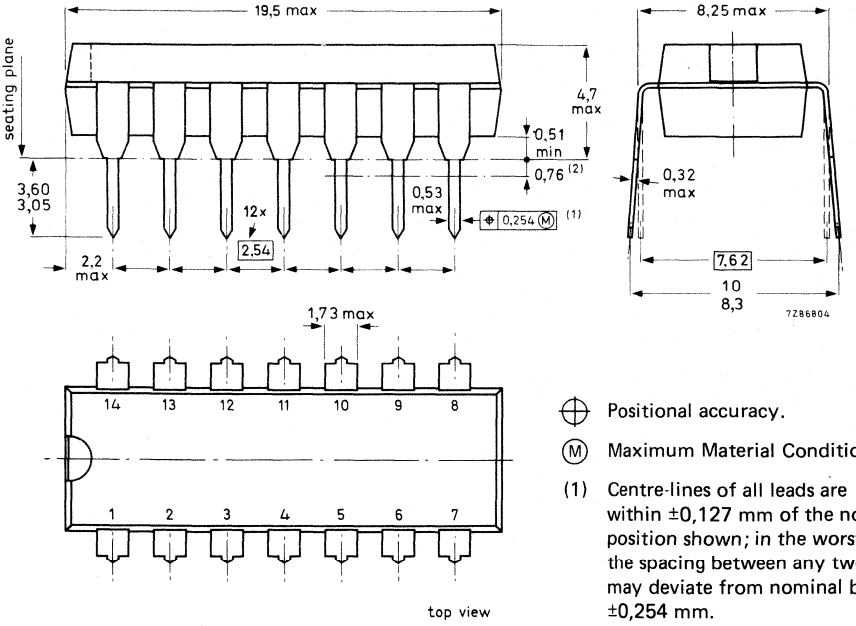
PACKAGE OUTLINES

CROSS-REFERENCE LIST: ICs TO PACKAGE OUTLINES

type number	description	package code	page
PCD3310P	20-lead DIL; plastic	SOT-146	438
PCD3310T	28-lead mini-pack; plastic	SO-28; SOT-136A	436
PCD3311P	14-lead DIL; plastic	SOT-27K, M, T	421
PCD3311T	16-lead mini-pack; plastic	SO-16L; SOT-162A	441
PCD3312P	8-lead DIL; plastic	SOT-97A	424
PCD3312T	8-lead mini-pack; plastic	SO-8L; SOT-176	443
PCD3315P	28-lead DIL; plastic	SOT-117D	431
PCD3315T	28-lead mini-pack; plastic	SO-28; SOT-136A	436
PCD3320P	18-lead DIL; plastic	SOT-102G	428
PCD3320D	18-lead DIL; ceramic (cerdip)	SOT-133A, B	434
PCD3321P	18-lead DIL; plastic	SOT-102G	428
PCD3321D	18-lead DIL; ceramic (cerdip)	SOT-133A, B	434
PCD3322P	18-lead DIL; plastic	SOT-102G	428
PCD3322D	18-lead DIL; ceramic (cerdip)	SOT-133A, B	434
PCD3323P	28-lead DIL; plastic	SOT-117D	432
PCD3323D	28-lead DIL; ceramic (cerdip)	SOT-135A	435
PCD3323T	28-lead mini-pack; plastic	SO-28; SOT-136A	436
PCD3324P	18-lead DIL; plastic	SOT-102G	428
PCD3324D	18-lead DIL; ceramic (cerdip)	SOT-133A, B	434
PCD3325A	18-lead DIL; plastic	SOT-102G	428
PCD3343P	28-lead DIL; plastic	SOT-117D	432
PCD3343D	28-lead DIL; ceramic (cerdip)	SOT-135A	435
PCD3343T	28-lead mini-pack; plastic	SO-28; SOT-136A	436
PCD3360P	16-lead DIL; plastic	SOT-38	422
PCD3360T	16-lead mini-pack; plastic	SO-16L; SOT-162A	441
PCD3361P	8-lead DIL; plastic	SOT-97EE	425
PCD3361T	8-lead mini-pack; plastic	SO-8L; SOT-176	443
PCD5101P	22-lead DIL; plastic	SOT-116	430
PCD5101T	24-lead mini-pack; plastic	SO-24; SOT-137A	437
PCD5114P	18-lead DIL; plastic	SOT-102G	428
PCD5114D	18-lead DIL; ceramic (cerdip)	SOT-133A, B	434
PCD5114T	20-lead mini-pack; plastic	SO-20; SOT-163A	442
PCD8571P	8-lead DIL; plastic	SOT-97A	424
PCD8571D	8-lead DIL; ceramic	SOT-151A	439
PCD8571T	8-lead mini-pack; plastic	SO-8L; SOT-176	443
PCF1251P	8-lead DIL; plastic	SOT-97A	424
PCF1251T	8-lead mini-pack; plastic	SO-8; SOT-96A	423
PCF2111P	40-lead DIL; plastic	SOT-129	433
PCF2111T	40-lead mini-pack; plastic	VSO-40; SOT-158A	440
PCF8570	8-lead DIL; plastic	SOT-97A	424

type number	description	package code	page
PCF8573	16-lead DIL; plastic	SOT-38	422
PCF8574P	16-lead DIL; plastic	SOT-38	422
PCF8574T	16-lead mini-pack; plastic	SO-16L; SOT-162A	441
PCF8576T	56-lead mini-pack; plastic	VSO-56; SOT-190	444
PCF8576U	uncased chip in tray		
PCF8577P	40-lead DIL; plastic	SOT-129	433
PCF8577T	40-lead mini-pack; plastic	VSO-40; SOT-158A	440
TDA7000	18-lead DIL; plastic	SOT-102HE	429
TDA7050T	8-lead mini-pack; plastic	SO-8; SOT-96A	423
TEA1042	24-lead DIL; plastic	SOT-101A	426
TEA1046	24-lead DIL; plastic	SOT-101A	426
TEA1060	18-lead DIL; plastic	SOT-102A	427
TEA1061	18-lead DIL; plastic	SOT-102A	427
TEA1075	18-lead DIL; plastic	SOT-102HE	429

14-LEAD DUAL IN-LINE; PLASTIC (SOT-27K,M,T)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

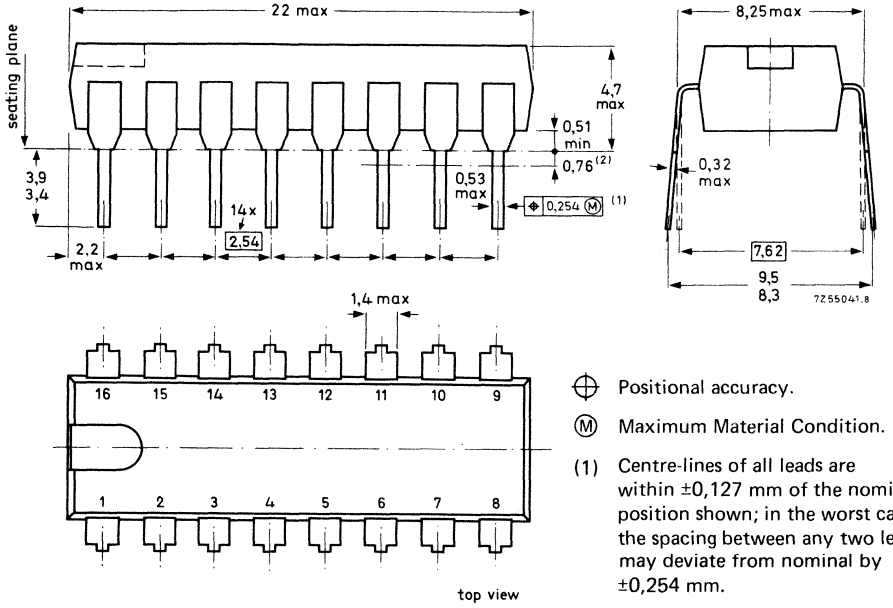
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

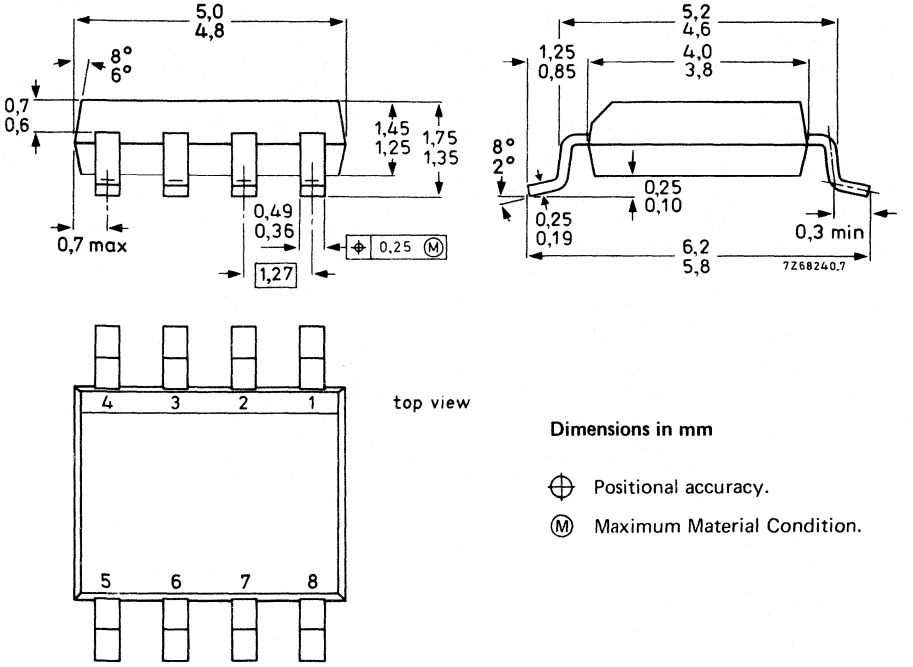
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

8-LEAD MINI-PACK; PLASTIC (SO-8; SOT-96A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

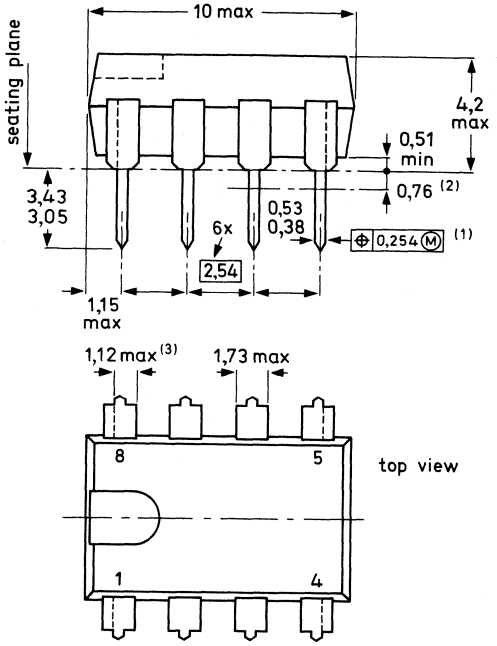
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

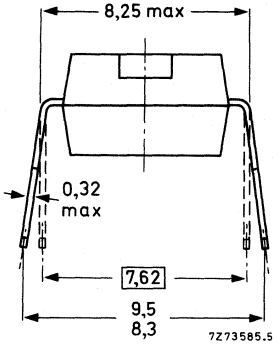
Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

8-LEAD DUAL IN-LINE; PLASTIC (SOT-97A)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

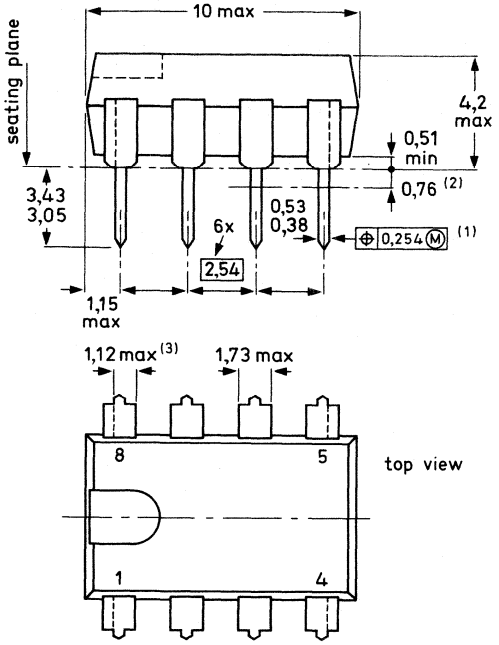
2. By dip or wave

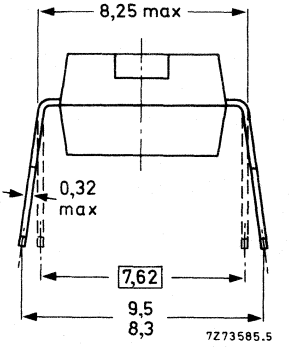
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

8-LEAD DUAL IN-LINE; PLASTIC (SOT-97EE)





Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

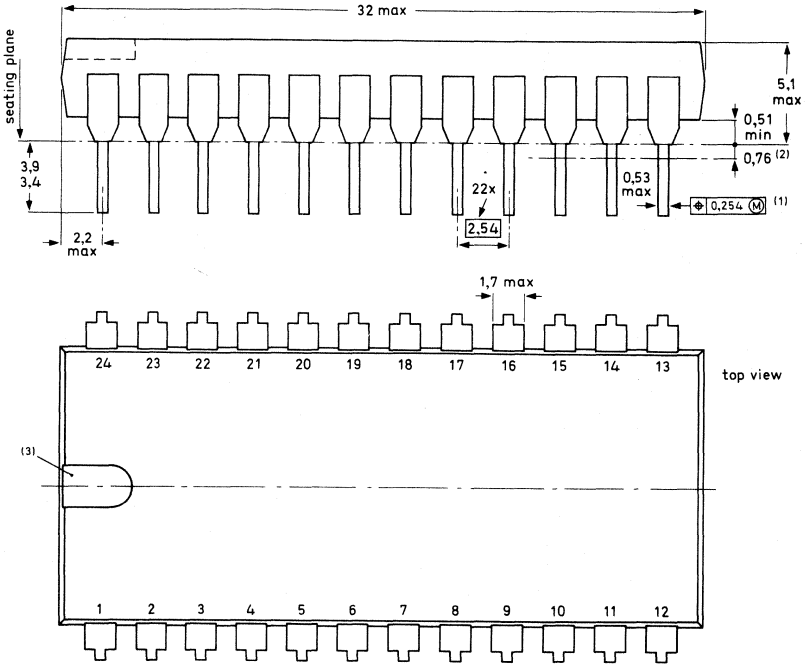
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

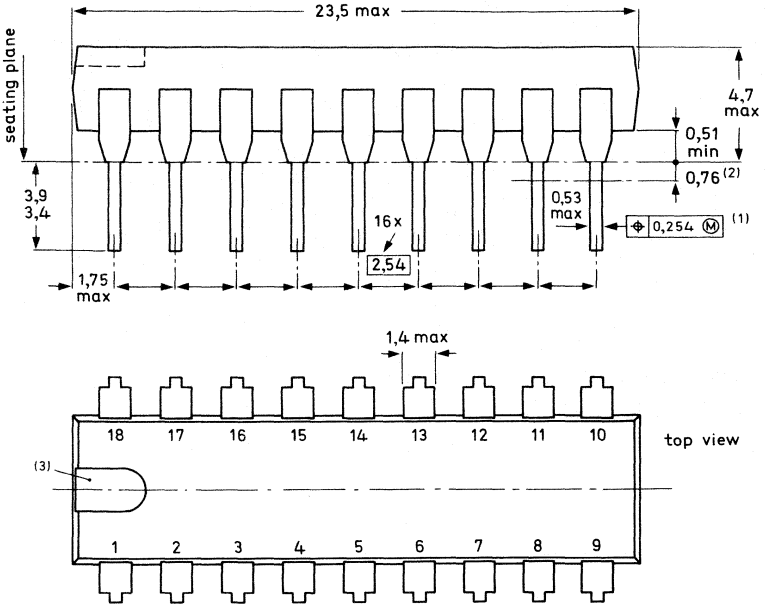
(3) Index may be horizontal as shown, or vertical.

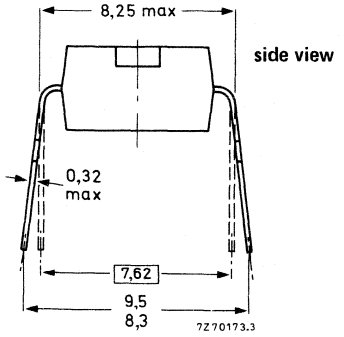
Dimensions in mm

SOLDERING

See SOT-27K, M, T.

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102A)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

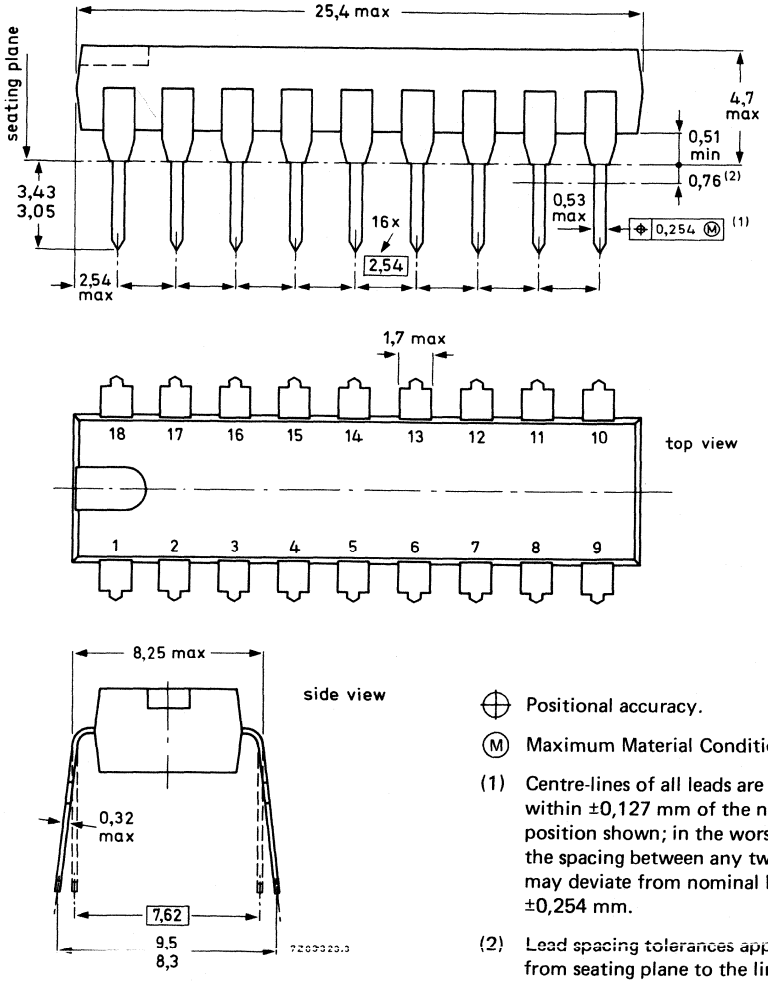
(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

See SOT-27K, M, T.

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102G)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

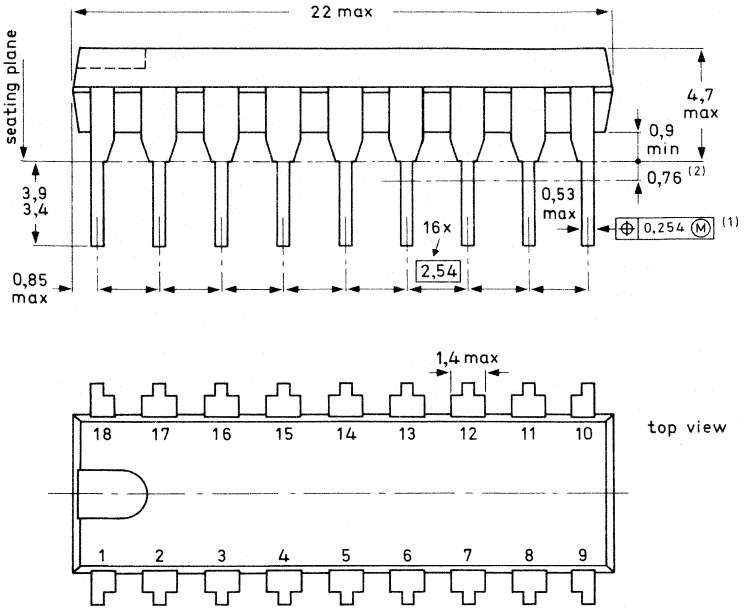
(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

See SOT-27K, M, T.

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102HE)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

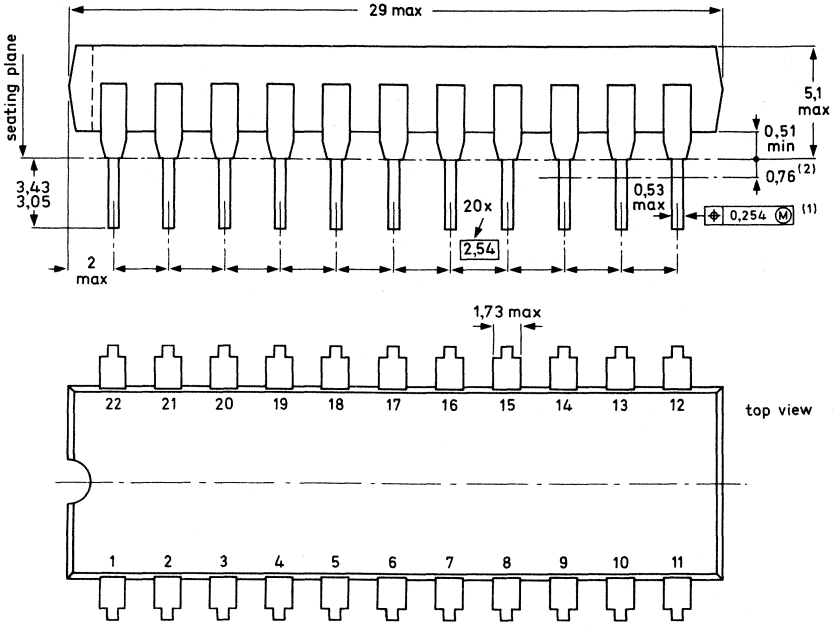
(2) Lead spacing tolerances apply from seating plane to the line indicated.

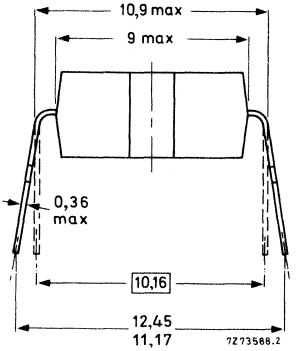
Dimensions in mm

SOLDERING

See SOT-27K, M, T.

22-LEAD DUAL IN-LINE; PLASTIC (SOT-116)





side view

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

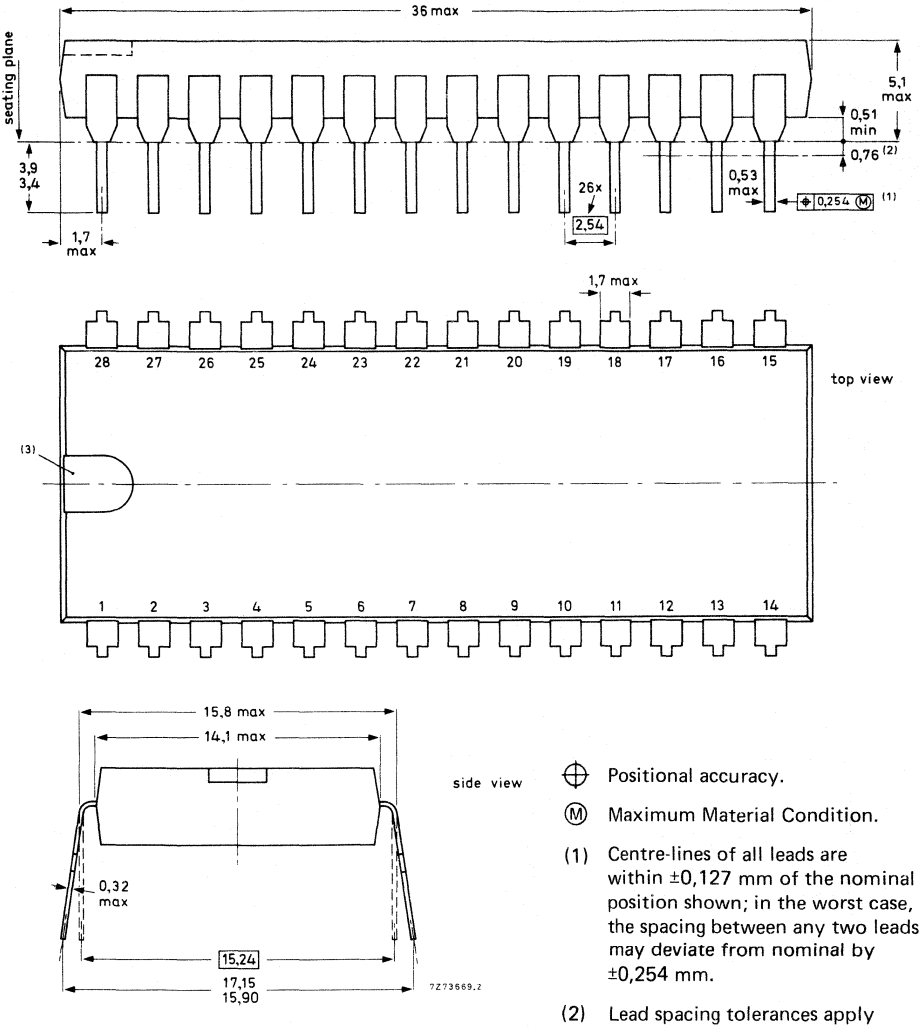
(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

See SOT-27K, M, T.

28-LEAD DUAL IN-LINE; PLASTIC (SOT-117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

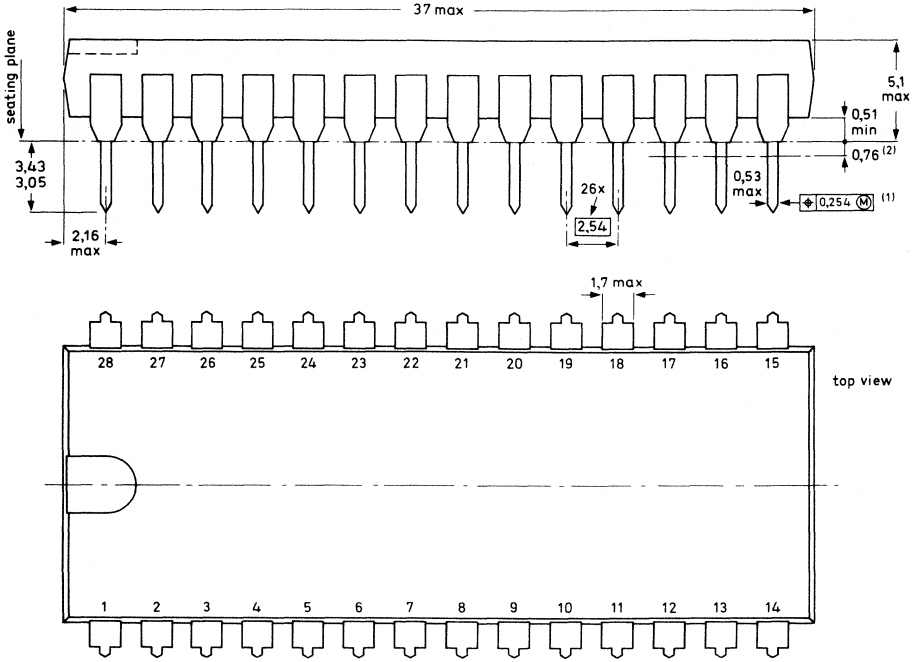
(3) Index may be horizontal as shown, or vertical.

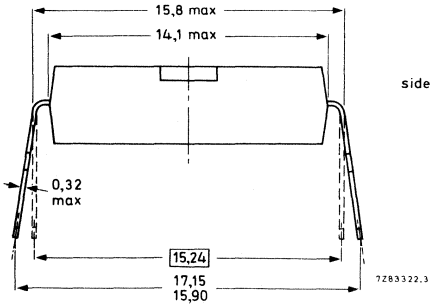
Dimensions in mm

SOLDERING

See SOT-27K, M, T.

28-LEAD DUAL IN-LINE; PLASTIC (SOT-117D)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

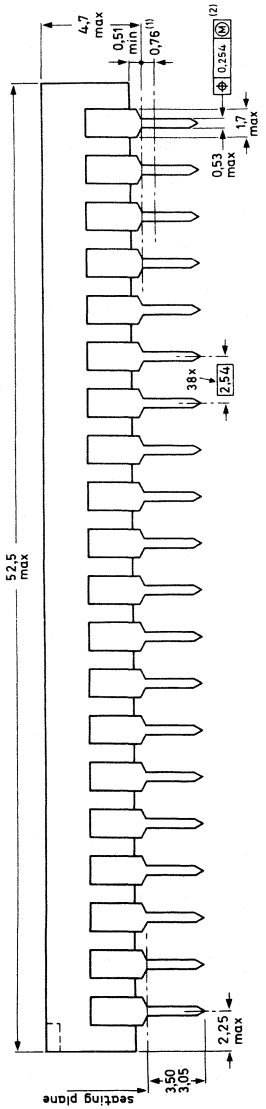
(2) Lead spacing tolerances apply from seating plane to the line indicated.

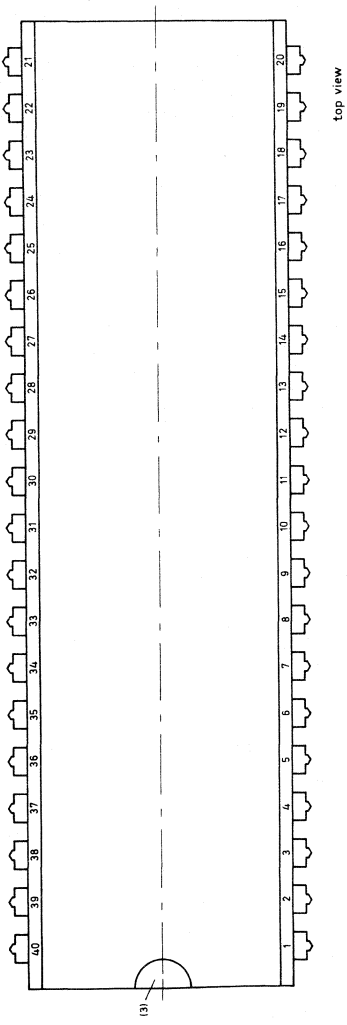
Dimensions in mm

SOLDERING

See SOT-27K, M, T.

40-LEAD DUAL IN-LINE; PLASTIC (SOT-129)





⊕ Positional accuracy.

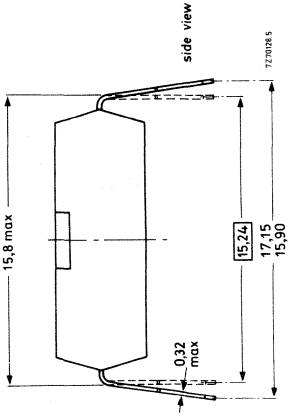
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

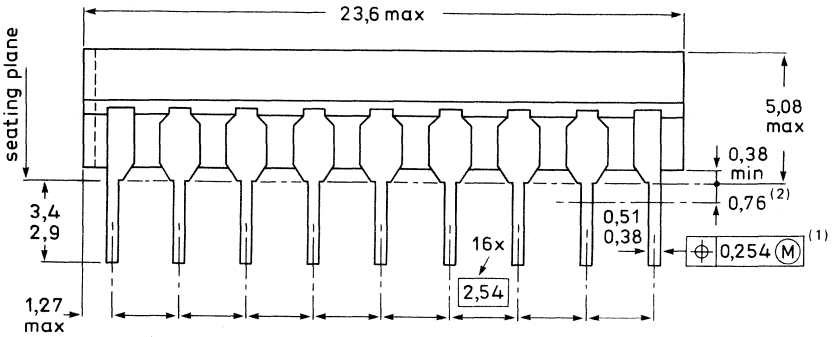
Dimensions in mm

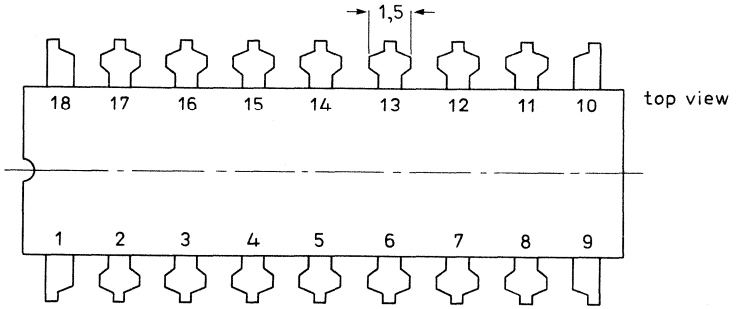


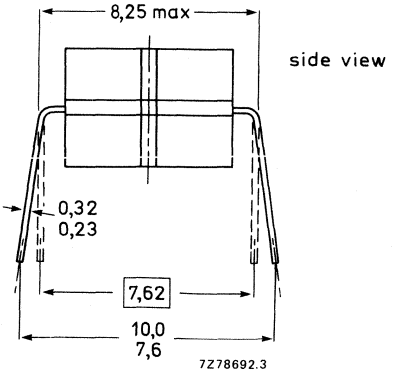
SOLDERING

See SOT-27K, M, T.

18-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-133A,B)







⊕ Positional accuracy.

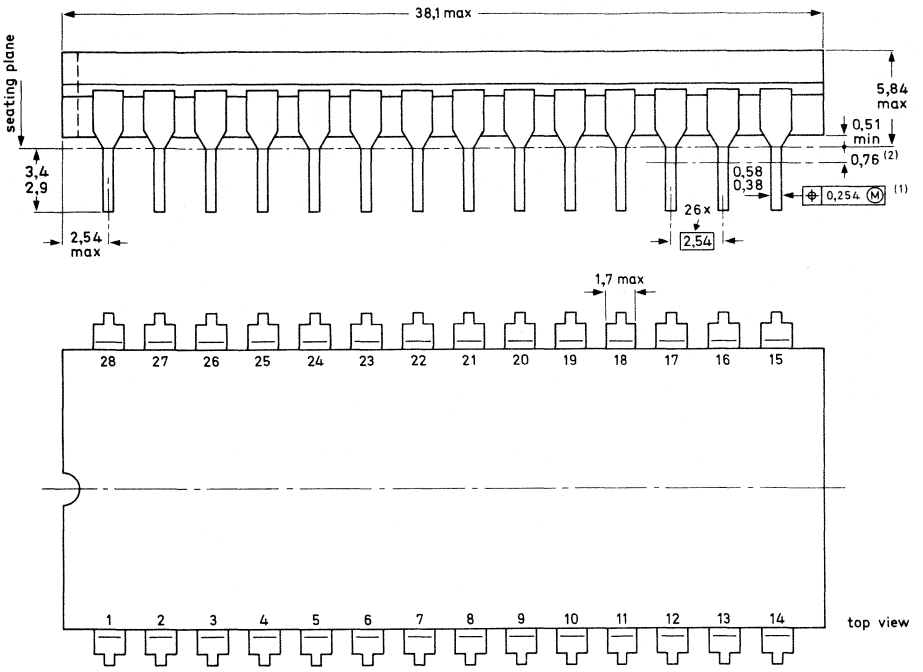
Ⓜ Maximum Material Condition.

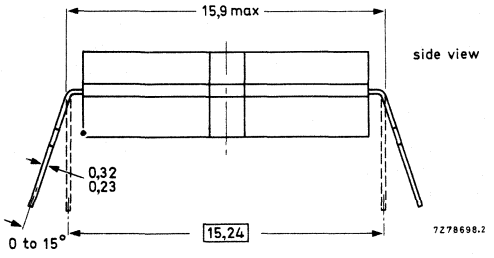
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-135A)





⊕ Positional accuracy.

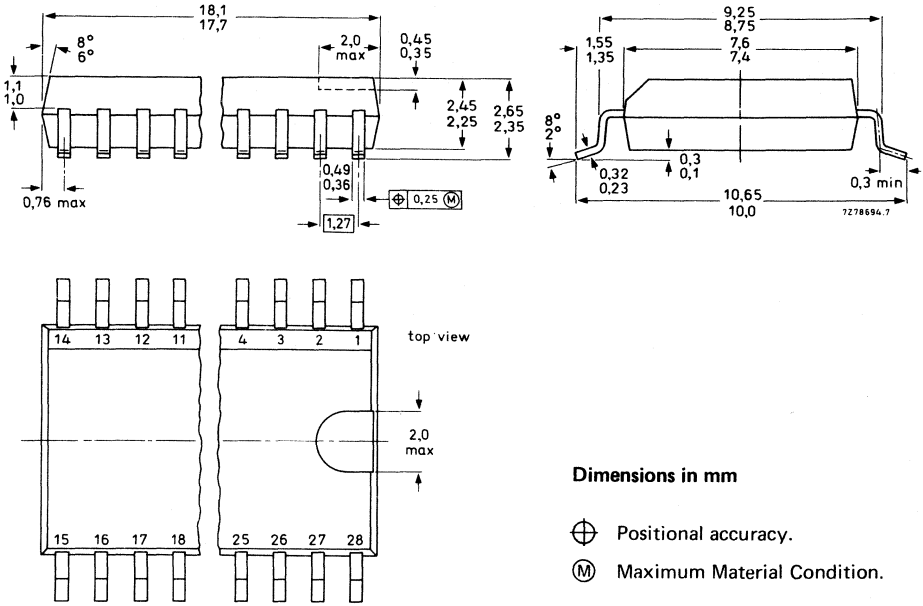
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD MINI-PACK; PLASTIC (SO-28; SOT-136A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

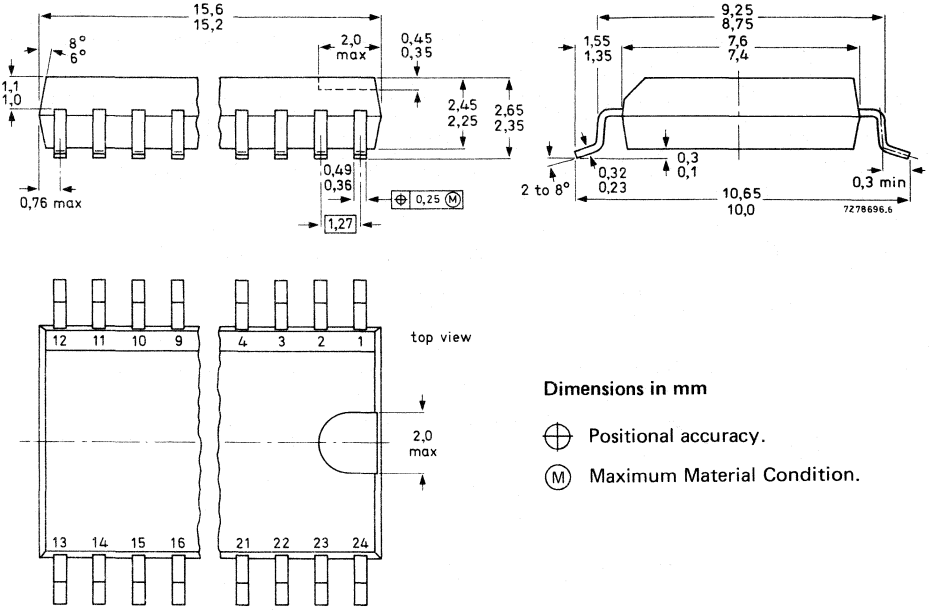
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

24-LEAD MINI-PACK; PLASTIC (SO-24; SOT-137A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

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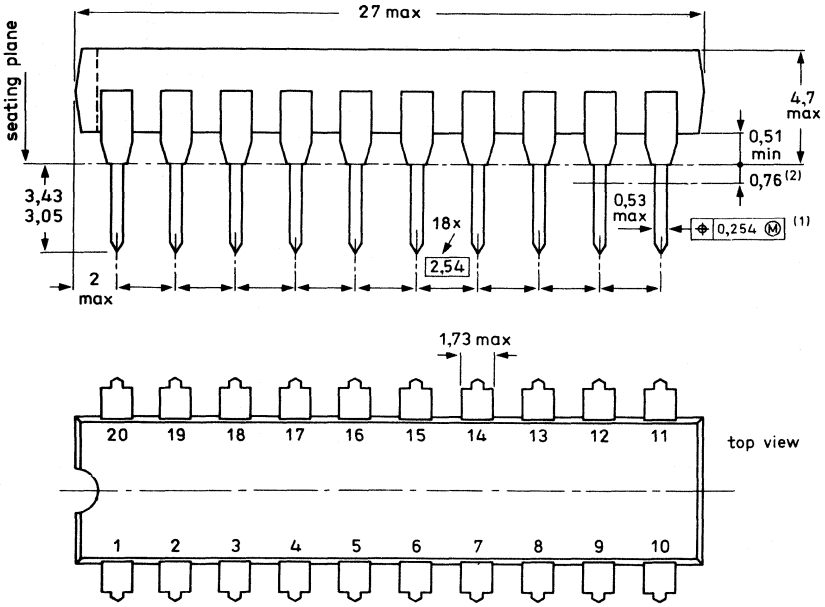
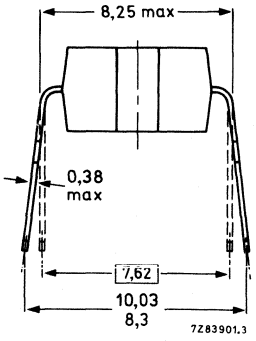
The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

20-LEAD DUAL IN-LINE; PLASTIC (SOT-146)





side view

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm

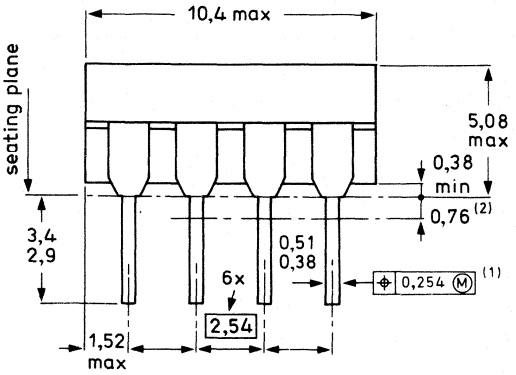
(2) Lead spacing tolerances apply from seating plane to the line indicated.

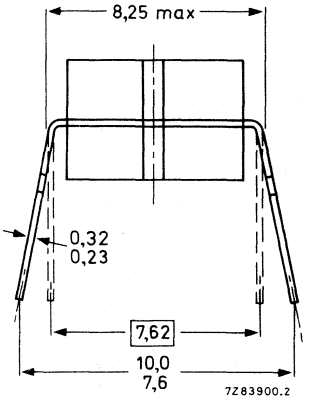
Dimensions in mm

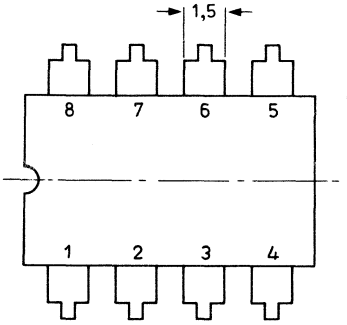
SOLDERING

See SOT-27K, M, T.

8-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-151A)







top view

⊕ Positional accuracy.

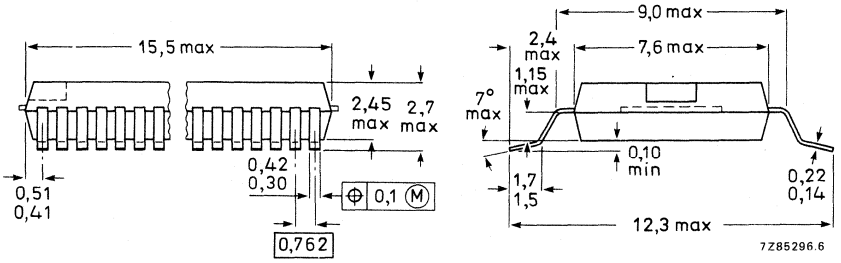
Ⓜ Maximum Material Condition.

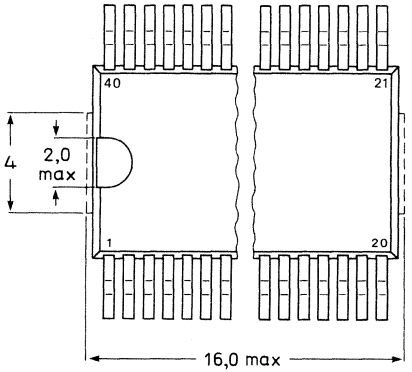
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

40-LEAD MINI-PACK; PLASTIC (VSO-40; SOT-158A)





Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

1. Soldering iron or pulse heated solder tool

Apply the heating tool to the flat part of the pin only.
Limit the contact time to maximum 10 seconds up to 300 °C, or 5 seconds up to maximum 400 °C.
When using the proper tools, all pins can be soldered in one operation within 2 to 5 seconds and 270 to 320 °C.

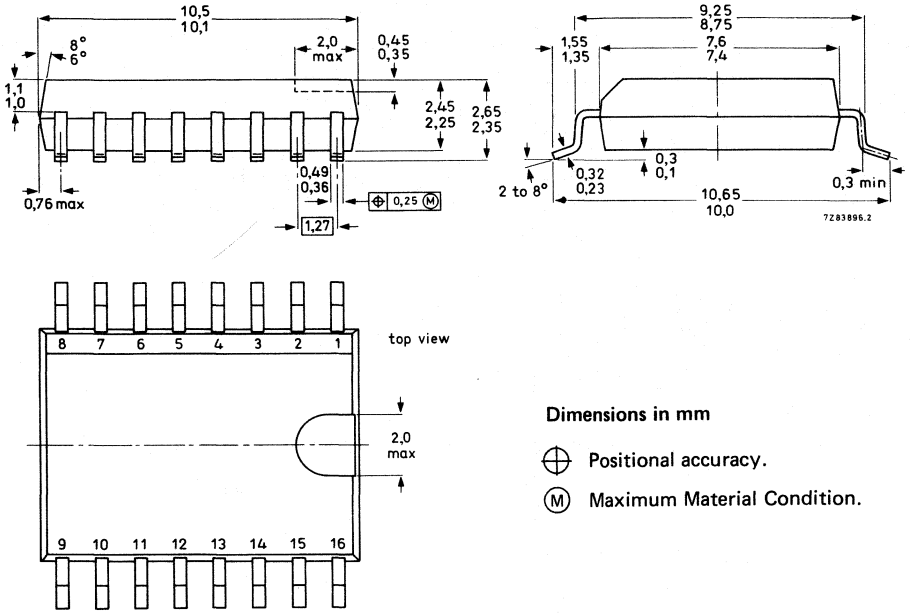
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C. The permissible total time of immersing the whole package in the bath is 10 seconds, if it is allowed to cool down to less than 150 °C within 6 seconds.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.
If the vertical part of the pin needs heating, reduce the soldering iron temperature to 260 °C.

16-LEAD MINI-PACK; PLASTIC (SO-16L; SOT-162A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

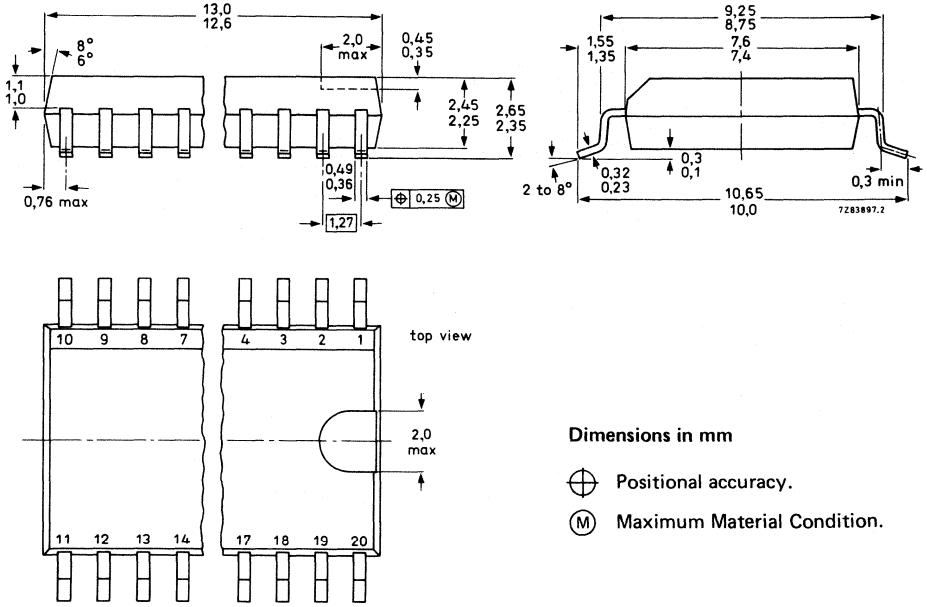
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

20-LEAD MINI-PACK; PLASTIC (SO-20; SOT-163A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

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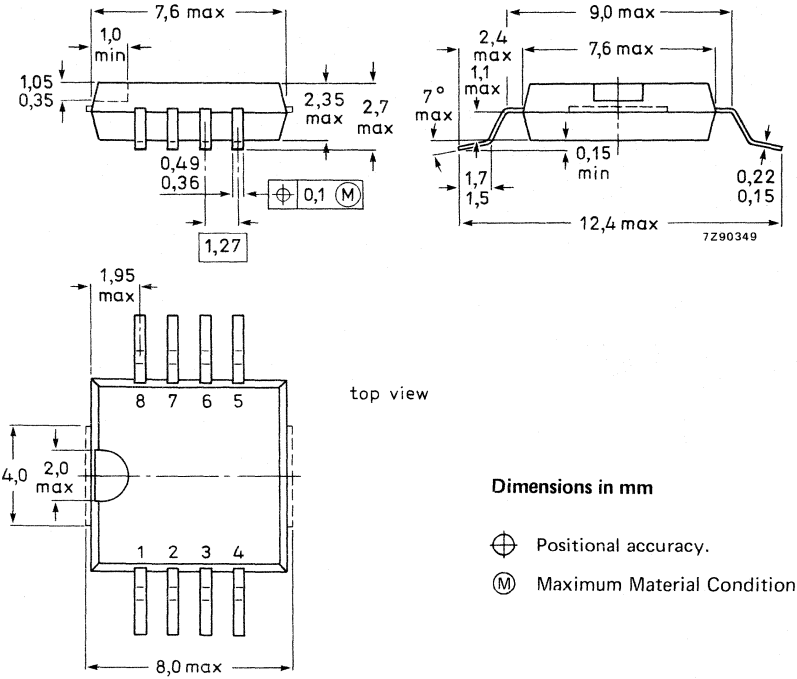
After soldering, the substrate must be cleaned of any remaining flux.

8-LEAD MINI-PACK; PLASTIC (SO-8L; SOT-176)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

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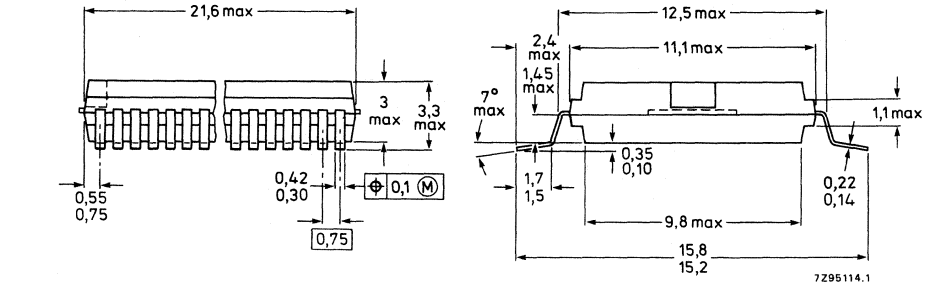
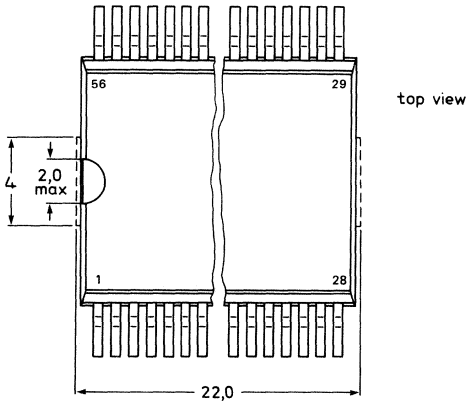
After soldering, the substrate must be cleaned of any remaining flux.

56-LEAD MINI-PACK; PLASTIC (VSO-56; SOT-190)





top view

Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

1. Soldering iron or pulse heated solder tool

Apply the heating tool to the flat part of the pin only.
Limit the contact time to maximum 10 seconds up to 300 °C, or 5 seconds up to maximum 400 °C.
When using the proper tools, all pins can be soldered in one operation within 2 to 5 seconds and 270 to 320 °C.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C. The permissible total time of immersing the whole package in the bath is 10 seconds, if it is allowed to cool down to less than 150 °C within 6 seconds.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.
If the vertical part of the pin needs heating, reduce the soldering iron temperature to 260 °C.

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